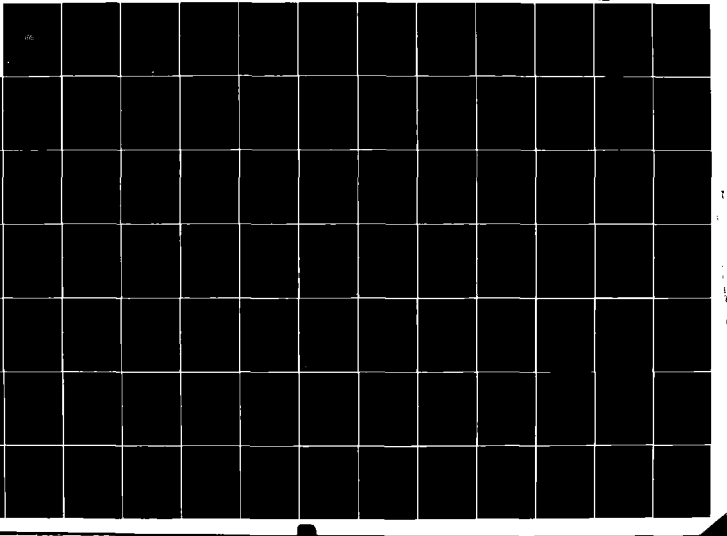
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MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
AUG 79 DAAK40-78-C-0290
UNCLASSIFIED HAC-PR79-18-669A NL

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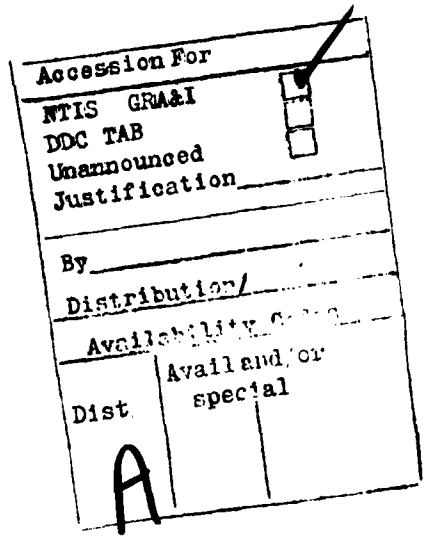
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20. ABSTRACT

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards containing complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the development of digital fault isolation methodology, and the identification of the corresponding optimum available automatic test hardware.

The subsequent contract option phase of this project involves the purchase, setup, and demonstration of the selected fault isolation hardware/software system, using the developed techniques.



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INTERIM REPORT – MM&T – DFI FOR PCBs – BASIC EFFORT

INTERIM REPORT

(BASIC EFFORT)

MANUFACTURING METHODS AND TECHNOLOGY FOR 'DIGITAL FAULT ISOLATION FOR PRINTED CIRCUIT BOARDS'

PROJECT NO. R783242

CONTRACT DAAK40-78-C-0290
25 AUGUST 1979
CDRL A003



FR 79-12-669A
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INTERIM REPORT (BASIC EFFORT)

Manufacturing Methods and Technology for 'Digital Fault Isolation for Printed Circuit Boards'

Project No. R783242

Prepared for

U.S. Army Missile Research and Development Command

Redstone Arsenal, Alabama 35809

Project Officer: G. Little
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Contract No. DAAK 40-78-C-0290
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Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

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FOREWORD

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards containing complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

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SECTION 1
OVERVIEW OF THE BASIC STUDY EFFORT

1. Program Objective and Summary of Study Results 1-0

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1. PROGRAM OBJECTIVE AND SUMMARY OF STUDY RESULTS

A direct objective of the DFI program is to select an optimum, commercial ATE system for advanced digital PCBs which is responsive to MIRADCOM MM&T. Through a comprehensive evaluation of D/PCB and ATE data bases, requisite performance and economic factors, the study has selected the Hewlett-Packard DTS-70 system.

Current nationwide production of digital PCBs for military and industrial electronic systems covers applications in missile guidance, fire control, radar, computer, communications, and displays. These systems contain complex, hybrid microelectronic components, various semiconductor logic families, dynamic memories, and microprocessors that are expected to continue into the 1980s. The diverse applications and the use of very large-scale integrated circuits (VLSI) in new systems, have made conventional PCB test and fault isolation largely ineffective. Furthermore, the increased cost of a PCB resulting from ineffective testing raises the investment in spares inventory.

The problem, shared by the military and industry, is to achieve efficient automatic test and fault isolation of digital PCBs both in production and field installations. In short, high throughput of operating PCBs and reduced production and inventory costs are continuing requirements.

By way of solution, this DFI program objective has been to establish the manufacturing methods and technology (MM&T) for applying a commercially available, state-of-the-art automatic test equipment (ATE) system, to test and fault isolate digital printed circuit boards (D/PCBs). The accompanying table summarizes the characteristics of the selected test system.

Program Highlights – During the 10 month basic study, effort concentrated on selection of an optimum ATE system that achieved efficient test and fault isolation to the minimum size component level. Required ATE system capability, with improvements for the Army's needs, is to include testing of large, complex D/PCBs of advanced design, containing LSI and microprocessor type circuit elements.

The DFI program basic effort result has selected the Hewlett-Packard DTS-70 ATE system for consideration by MIRADCOM for MM&T application to D/PCB test and fault isolation, and implementation in the succeeding 11-month hardware option. This selection was achieved by a comprehensive, objective evaluation of DFI pertinent ATE system factors.

Major tasks of the basic effort defined by Technical Requirement E0035 were structured into milestones of a program approved test plan presented in CDRL A008. Effort to select the ATE system was carried out by six tasks identified as:

- D/PCB Survey
- FI Test System Survey
- Performance Evaluation
- Testability Investigation
- DFI Methodology
- Select Test System (ATE)

Baseline equipment for study rapidly evolved into a set of 21 D/PCBs (derived from 6 prime military systems), and 7 primary test system candidates. Extensive parameter and other data were recorded and reduced for the baseline equipment with computer aided data handling. Applicable literature and military ATE data banks were actively researched.

Circuit Survey – A D/PCB questionnaire was derived to develop a computer data file for the D/PCB Survey. Containing 186 data items, the questionnaire covered D/PCB identification, digital, stimulus, and measurement parameters.

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Tester Survey – Similarly, the Test System Survey developed a computer data file through a tester questionnaire of 275 data items covering digital parameters, adapter, software, maintenance, and support.

Performance Evaluation – In the Performance Evaluation Task, D/PCB test requirements and test system capability (to meet requirements) were correlated by computer matching algorithms for percent achievement only of digital parameter compatibility (DPC). A match of 20 parameter groups for each D/PCB tester resulted in the test system rank for digital parameter matching. Test system selection criteria further combined test system DPC rank with software, test programming, tester hardware features, and maintenance-support using various weighting factors (Attachment III) and formed the composite system rank.

Testability Results – From the Testability Investigation, logic circuit analysis of the MIRADCOM Digital Autopilot PCBs yielded an average 17 percent improvement in testability.

DFI Methodology – Software required to handle test documents and production data base management for any test system were examined by the DFI Methodology. After final test system selection, a specific methodology flow diagram was outlined for the selected test system.

Data Verification – System data received by Hughes were verified in technical conferences at each supplier's plant. At the same time a practical system performance test was carried out using a test circuit with appropriate test program software for each system. This test measured system simulator software and test diagnostic performance with 5 predetermined circuit faults.

System Scoring – The verified system data determined a revised composite rank score. The verified composite rank score, relative D/PCB programming cost, and the quoted system cost-performance performance evaluation were further combined to form the theoretical system selection score. Beyond the theoretical system selection, evaluated results of the practical system performance test established measured scores for the system simulator software, and fault diagnostic capability.

Final Selection – In the final system selection, a weight of 75 percent was assigned to the system theoretical score and 25 percent to the performance test score. From these two scores the system that achieved the largest total score of 1514 points is the HP DTS-70.

Within initially stated economic bounds, the DFI study recommends for production testing of D/PCBs the HP-DTS-70 with characteristics and major features shown in the table.

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MAJOR CHARACTERISTICS OF THE SYSTEM SELECTED BY THE DFI STUDY FOR D/PCB PRODUCTION TESTING

Item/Parameter	Characteristic
System Supplier, Model	Hewlett Packard DTS-70
I/O Pins	360
Digital Driver/Receiver	± 15V Programmable
UUT Logic Families	Mixed
Logic Simulator	Testaid III
Test Pattern Rate	> 10 kHz per pin
Clock	5 MHz
Diagnostic Probe	Computer guided, operator prompts
Fault Isolation	IC or component
Software Language	FORTRAN IV, Testaid
Peripheral	
Memory	19.6 M Byte (7906/020)
Terminal	CRT, Keyboard (2645)
Line Printer	400 L/M (2608A/210)
Power	115 VRMS 50-60 Hz
System	± 10, ± 20 ± 40 VDC
UUT	programmable 5V fixed
General	
Temp	40°C max
Size	65 h x 99 w x 46 d
Construction	Rack

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0. DEFINITION AND RELATIONSHIP OF BASIC EFFORT TASKS

The Digital Fault Isolation of printed circuit board program tasks were defined by TR E0035 for the 10 month basic effort. The freedom to develop parallel and sequential tasks enabled Hughes to coordinate manpower utilization within the schedule milestones.

A functional plan of the Digital Fault Isolation (DFI) program 10 month basic study effort, outlined by TR E0035, appears in the figure on the opposite page.

Effort required in each of six major tasks was based on a second iteration estimate of the number of D/PCB samples, types of contributing military systems, and the number of test systems to be surveyed and tabulated.

Subsequently, at the beginning of the program, a task plan, CDRL 008, was developed, reviewed, and approved by MIRADCOM. Each task of the plan detailed its objective, subtasks, key milestone, and manpower effort.

During the course of each task, detailed supporting information and data were compiled, which are separately identified by task and appear in Attachments I through IV of this report.

A definition of tasks and their relationship as performed during the basic effort follows.

Task 1 – D/PCB Survey – The first task was to originate a D/PCB questionnaire and develop a computer data file of detailed test requirements for MIRADCOM and Hughes PCBs.

Task 2 – FI Test System Survey – The next task originated a tester questionnaire and developed a computer data file of tester characteristics and detailed test capabilities of test systems. Compiled tester data included digital parameters, adapter, software, maintenance, and support.

Task 3 – Performance Evaluation – Test requirements were correlated, by means of computer matching, for each D/PCB with test capabilities in each test system. The highest rank test systems were selected for final evaluation.

Task 4 – Testability Investigation – Current Government and military agency testability efforts were examined and military specifications were reviewed to derive a set of recommendations for testability in MIL standards.

A literature search of testability articles was evaluated and resulted in a Testability Design Guide. Logic circuits of MIRADCOM Digital Autopilot PCBs were examined and testability recommendations made to raise their testability.

Task 5 – DFI Methodology – Software required to handle test documents and production data base management for any test system were examined by the DFI Methodology. After final test system selection, a specific methodology flow diagram was outlined for the selected test system.

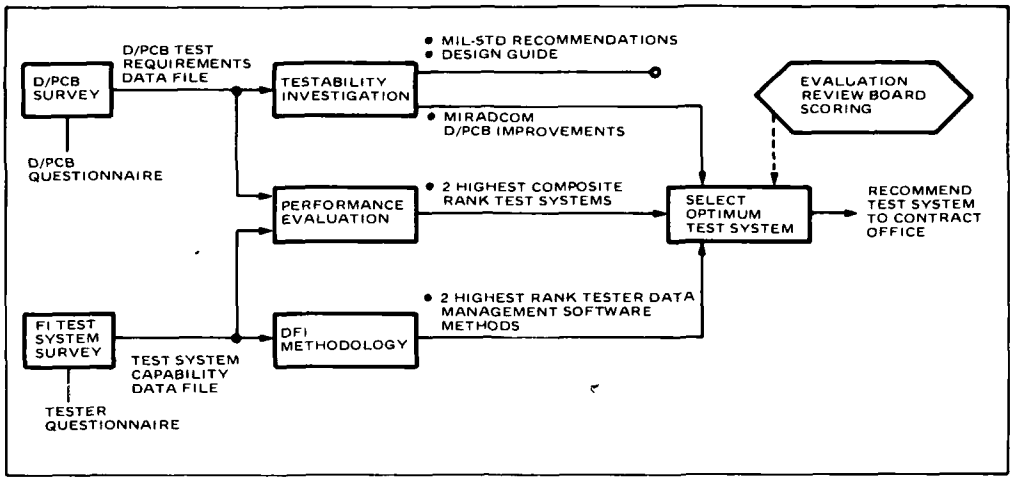
Task 6 – Select Test System – The highest ranked test systems were evaluated and scored by a review board for final test system selection and recommendation to MIRADCOM.

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DFI Basic Study Effort Task Development and Relationship. A presentation to MIRADCOM on the optimum system selected in the basic study was conducted during the third quarterly review held at Hughes.

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1. RESULTS OF THE DIGITAL PRINTED CIRCUIT BOARD (D/PCB) SURVEY

The digital test requirements that a test system has to satisfy were defined by surveying 21 D/PCB samples. A computer file of the data was then prepared for use during the performance evaluation phase of tester selection.

The groundwork necessary to prepare for an effective test system survey included first the development of test criteria, review of systems that use D/PCBs, preparation and issuance of a D/PCB questionnaire, and the conversion of the questionnaire responses into a D/PCB test requirements summary report.

Test Requirement Overview – Test system manufacturers design systems for specific types of testing. The driving concern is, of course, cost. Test systems with multiple test capabilities cost more than those that are designed for a particular type of test. Since the cost window for test system procurement was pre-defined for this study, it was necessary to create a set of bounding test criteria which would satisfy the testing requirements within the cost constraints. Table I shows the complete list of test boundaries which was used to limit the test system requirements for this study.

Item 1 in Table I shows the necessary and appropriate assumptions regarding pretest conditions. Only those active components which are MIL-STD-Class B rated and are burned-in, as well as completely inspected, are allowed. Passive components may be burned-in and inspected as required. The bare PCB should be tested for errors prior to component insertion. At this time, the D/PCB should pass In-Circuit Component Inspection and Test (ICCIT) to assure that all components have been installed correctly and that there are no shorts or opens on the PCB.

Once the ICCIT has been passed, the D/PCB is ready for the main subject of this study, namely, functional testing and fault isolation of D/PCBs. A limitation on the types of functional testing was also required. Functional test of a D/PCB at real-time-clock rates and parametric test of components already inserted into a PCB are very costly items. At the present time, few, if any, test systems can provide either of these capabilities. The requirements for these tests should be restricted to special cases only and, in this light, the extended capability can be added to the adapter. In addition to D/PCB functional testing as limited above, each test system considered had to fault-isolate detected failures to a defective component level.

Questionnaire Development and Preliminary Systems Survey – With the test criteria established, two tasks were undertaken simultaneously as shown in the facing figure. A questionnaire was generated that would ask of any D/PCB, the necessary questions to identify its test requirements. Also, many different types of electronic systems were examined for D/PCB samples that would provide a wide range of technology and complexity.

The D/PCB questionnaire (see Attachment I, Section A) established requirements such as power, voltage, quantity of input/output pins, quantity and types of components, clock rates, input/output signal types, and the number of loops on the board.

The survey of electronic systems resulted in the selection of 21 D/PCB samples that represented missile systems, radar systems, display systems, data processing systems and computer systems. Table II shows a complete list of the 21 D/PCB samples organized by the system from which they were selected. It also gives a sample of the logic that exists on the D/PCB.

When the D/PCB questionnaire was completed for each of the 21 D/PCB samples it provided a complete list of test requirements that a test system should

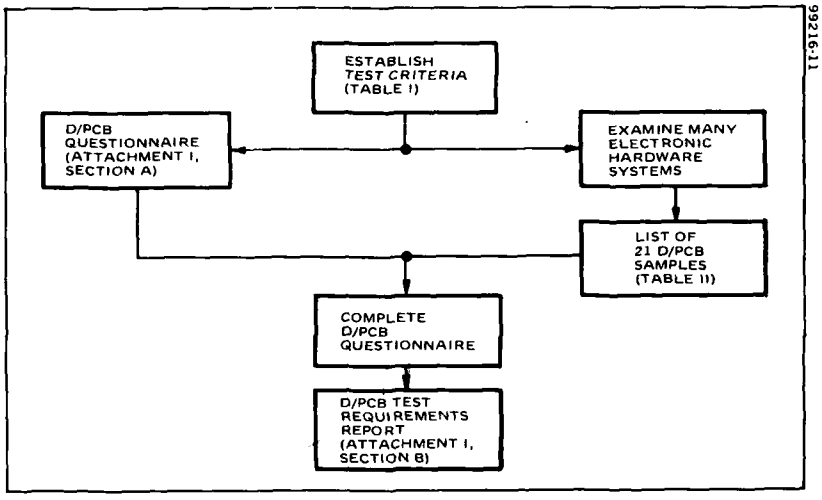
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be able to satisfy. The information was then entered into a computer data file. This data file was used as a reference for the D/PCB test requirements/tester capability matchup computer program. A complete summary report of the test requirements for all 21 D/PCB samples was generated and is included as Attachment I, Section B.



D/PCB Survey Procedure. Test criteria, D/PCB questionnaire, and a list of 21 D/PCB samples were used to establish the test requirements for the test system.

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1. RESULTS OF THE DIGITAL PRINTED CIRCUIT BOARD (D/PCB) SURVEY (Continued)

TABLE I. D/PCB TEST CRITERIA

Test Item	Required Yes/No	Remarks
1. Pretest Conditions		
1.1 Burn-in	Yes	Active components – 100% MIL-STD-Class B Passive components – as required
1.2 Receiving inspection	Yes	Active components – 100% Passive components – per standard sampling
1.3 Bare board test	Yes	All boards
1.4 ICCIT (in-circuit component inspection and test)	Yes	All assemblies
2. Functional testing		
2.1 Functional static	Yes	Combinational logic per truth table as required
2.2 Functional dynamic (not real time)	Yes	Sequential logic per truth table as required
2.3 Functional dynamic (real-time-clock)	No	Except special cases
3. Parametric testing		
3.1 Static parametric	No	Except special cases
3.2 Dynamic parametric	No	Except special cases
4. Environmental testing	No	Except in rare special cases
5. Fault isolation	Yes	To defective component level

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TABLE II. D/PCB SAMPLES AND SYSTEM SOURCES

System	Circuit Card Part Number	Description	Logic Types
MIRADCOM Autopilot		Missile System	
	390037	Digital Autopilot No. 1	LATCH, AOI, PROM, F/F, RAM
	390038	Digital Autopilot No. 2	Microprocessor, RAM, PROM
	390039	Digital Autopilot No. 3	Register, MUX, CNTR, F/F, SR
	390040	Digital Autopilot No. 4	CNTR, Decoder, OPAMP
Phoenix		Missile System	
	D3567251	Program memory	PROM, Decoder, Program memory
AWG-9/ AIM-54		Phoenix Missile System F-14	
	3523201	Arithmetic unit	MUX, Multiplier, SR, X-OR, ALU
	3567221	Discrete fourier transform	ROM, ALU, QUAD-TO-POLAR Processor, Multiplier, S and H
HMD-22		Navy display system	
	1633050	16-bit microprocessor	Microprocessor (4); 139 ICs
JTIDS		Joint Tactical Information Distribution System	
	1650036	Decision logic multinet	Adder, F/F, MUX, RAM, ROM, CNTR
	1650038	Reed Solomon encoder	RAM, ROM, SR, X-OR, MUX
	1650039	Reed Solomon decoder	ALU, ROM, F/F, RAM, CNTR
AN/UYQ-21		Navy Display System	
	1640302	Micro controller	2048 Bit ROM, Addressable latch SR, data selector/MUX, F/F, Gates
	1646310	32K-16 RAM	RAM, GATES, DECODER, DE MUX
	1646333	Arithmetic register	4 bit microprocessor, X-OR data selector/MUX, carry generator, AND-OR
	3177422	131072 Bit Memory	RAM, Gates
AN/TPQ-36/37		Mortar, Artillery Locating radar	
	1635883	Computer message control	F/F, PROM, Decoder, X-OR, MUX
	1635884	Clock/TV sync generator	CNTR, PROM, F/F, ONE-SHOT
	1635910	Doppler filter	F/F, CNTR, FULL ADDER, TRI-STATE, Register, Multiplier
	1635918	Pulsed interference detector	F/F, Bi-directional SR, CNTR, MUX, Adder, MAG COMP
	1635972	Microprocessor	Microprocessor (MC 8080 A/B)
	1642182	Memory (8192 word x 18 bit)	RAM

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1. OVERVIEW OF THE FAULT ISOLATION TESTER SURVEY

A test system questionnaire was prepared and issued for each primary test system candidate which had been identified during a survey on military ATE Data Banks and commercial digital tester manufacturing. Response data were then compiled for use during the evaluation phase of tester selection.

The major steps in the tester survey plan, beginning with the data search and ending with the capability summary report, are shown in the figure on the opposite page.

To formulate a comprehensive Digital PCB tester questionnaire, a literature search on available ATE was conducted during the early phase of the project. The literature sources included the Technical Abstract Bulletins from the Defense Documentation Center, Scientific and Technical Aerospace Reports from NASA, Government-Industry Data Exchange Program (GIDEP), Hughes Aircraft Company's Information Research (dialog on-line retrieval service), IEEE Semiconductor Test Conference Proceedings, IEEE AUTOTESCON Conference Records, and Industry/Joint Services Automatic Test Conference and Workshop Proceedings.

The tester questionnaire was developed to quantitatively identify characteristics or features of each test system in 5 categories: 1) general, i.e., test pattern frequency, maximum of available drivers/sensors for connection to UUT, etc. 2) digital test, 3) test fixture, 4) software, and 5) maintenance and support (see Attachment II, Section A). The tester manufacturer responses to the questionnaire on digital test features were recorded in the computer data file and were used at a later date to match against the digital PCB test requirements surveyed for this project. A Test System Summary Report (Attachment II, Section B) was generated to include testing capabilities of all seven testers.

To evaluate all the D/PCB testers available in the military inventory, an extensive survey was made of the three following ATE data banks: The U.S. Army Central TMDE Activity at Lexington, Kentucky; the San Antonio Air Logistic Center at Kelly AFB, Texas; and the Naval Air Engineering Center at Lakehurst, New Jersey. Additionally, to include other D/PCB testers, a survey was made of all available systems from commercial tester manufacturers.

The information extracted from the ATE data bank survey and the commercial tester manufacturers survey provided an extensive list of potential production digital printed circuit board testers for initial consideration.

The next step was to establish a set of criteria that would narrow the field down to a reasonable number of testers for evaluation. The test systems selected as the primary candidates were required to meet the following criteria: 1) perform a functional test of a D/PCB. The PCB testing criteria discussed in Topic 2A-1 will complement and support this criterion. 2) Provide high performance, which includes the system testing capability and hardware/software performance. 3) Be a proven factory test system, currently used by industrial and military organizations. 4) Provide established maintenance and logistic support. It is very important that the tester manufacturer provide the necessary maintenance and logistic support for the test system. Service availability, self-test capability, and dependability are important features required to keep the test system operational. 5) Be able to grow and expand for future testing requirements. This could include features such as multi-terminals, I/O pins expansion, memory size expansion, and modular software. 6) Be cost effective. The test system initial procurement cost was set at about $145,000 by agreement with the contract office.

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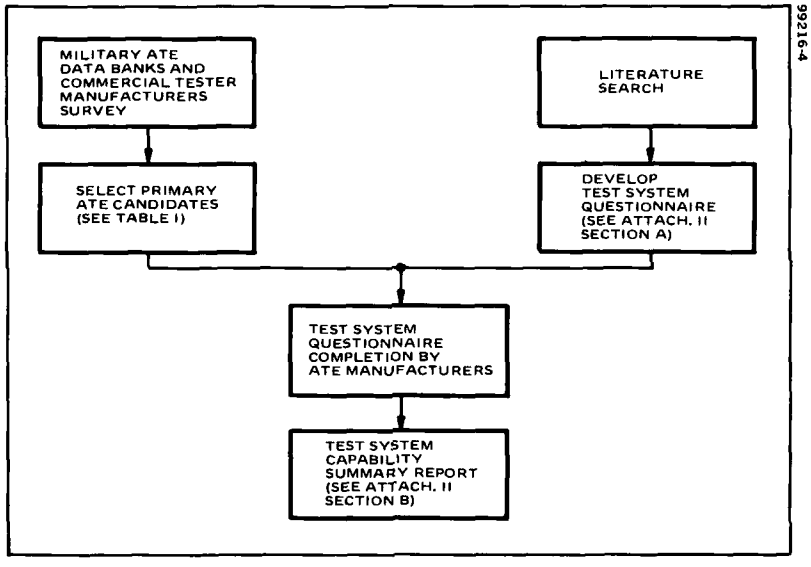
There are seven primary candidates that will probably meet the cost constraint and the rest of the criteria mentioned above. The alternate candidates are testers that would cost over $200,000, but will satisfy most or all of the first four criteria mentioned. The preselected primary tester candidates and the alternate tester candidates are shown in Table I and Table II.

TABLE 1. DIGITAL FAULT ISOLATION ATE SYSTEMS (PRIMARY CANDIDATES)

Manufacturer	Model
Computer Automation	4400
Fluke Trendar	3040A
General Radio	1795
Hewlett-Packard	DTS-70
Trace Instruments	TL-8
Teradyne	L-135
Texas Instruments	ATS-960

TABLE II. DIGITAL FAULT ISOLATION ATE SYSTEMS (ALTERNATE CANDIDATES)

Manufacturer	Model
General Radio	1796, 1799
Hewlett-Packard	3060A
Instrumentation Engineering	390
Optimized Devices	6000
Tektronix	S-3260, S-3280
Watkins Johnson	1300, 1500



Test Survey Plan. The initial tester survey resulted in a list of primary ATE candidates which were examined for their capability. The results were compiled into a capability summary report.

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1. CORRELATION OF TEST REQUIREMENTS WITH CANDIDATE TEST SYSTEM CAPABILITIES

Five computer programs were developed to process the large data files and to perform an objective comparison of D/PCB test requirements with candidate test system capabilities. Test systems were ranked by percent achievement on all D/PCBs, providing a digital parameter compatibility score used in further test system evaluations.

The parts of the Performance Evaluation (PE) task are itemized in the table below and described in this subsection.

Application of computer methods was necessary for most of the PE task to reduce time and effort, and to avoid data errors in dealing with the extensive data and large data files presented by 21 D/PCBs and 7 test systems.

Accordingly, two experienced programmers, working with Fortran IV and an IBM 370, developed five main programs which record and manipulate D/PCB and test system data. The programs, shown in Figure A, are as follows:

- Print PCB Tester Questionnaire
- Input PCB Tester Data
- Report PCB Tester
- Matchup PCB Tester
- Results PCB Tester Matchup Report.

Print PCB Tester Questionnaire – This program prints out blank questionnaires for either digital PCBs or digital testers. Details of the questionnaires appear in Section A of Attachment I and II. There are 179 PCB parameters and 173 tester parameters which are separated into 24 parameter groups. Each PCB group was matched to its corresponding tester group, parameter by parameter. Some of the parameters are not used in the matching algorithms as they are for information only.

The tester questionnaires were sent to seven manufacturers. When returned, they were checked for completeness and accuracy.

PCB questionnaires for 21 selected cards were completed at Hughes.

Input PCB Tester Data – The second program is used to store data in the computer. It prompts the user with the questions that are on the questionnaire. The user types-in the data which is then stored in either the Digital Tester Data or Digital PCB Data permanent data file. These files are used by the Report program and the Matchup program.

Report PCB Tester – The third program is used to printout a summary report for each tester and each PCB. It prints a completed questionnaire which is used for verification of input data and final copies of individual tester and PCB input data. Details of the PCB or tester report appear in Section B of Attachment I or II.

PERFORMANCE EVALUATION SUBTASKS

Subtask	Described in Topic
• Explanation of digital parameter correlation	(This Topic)
• Overview of digital parameter matchup (DPC) report	2.C-2
• Overview and evaluation of non-digital factors	2.C-3
• Tester composite ranking and selection of two final tester candidates	2.C-4

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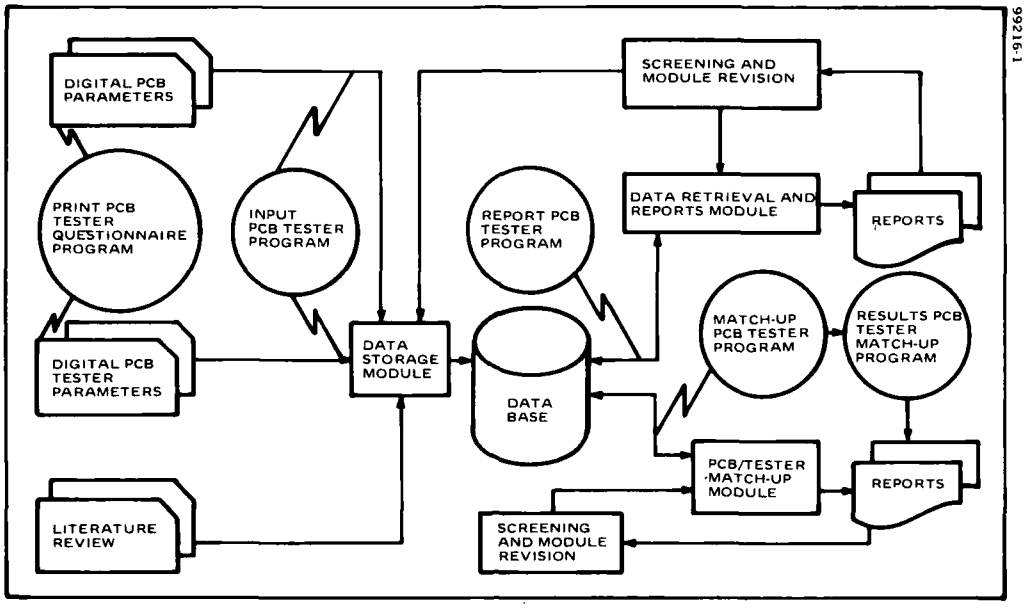


Figure A. Automatic Processing of PCB and Tester Data. Five main programs were developed with FORTRAN IV and an IBM 370 to record and manipulate D/PCB and test system data.

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1. CORRELATION OF TEST REQUIREMENTS WITH CANDIDATE TEST SYSTEM CAPABILITIES (Continued)

Matchup PCB Tester – A fourth main driver program reads, controls, and organizes the data from the Digital Tester Data and Digital PCB Data files. As shown in Figure B, the program sends the information for the first tester and the first PCB to the digital matching algorithms, where the data are compared and any tester shortcomings are recorded.

A CRITICAL shortcoming is recorded if all tester parameters in a group failed to meet the PCB's parameter requirements for that group. A CONDITIONAL shortcoming is recorded when an individual parameter within a group failed. When completed, a tester thoroughness percentage (achievement) is calculated for the PCB.

The tester is then sent through the matching algorithms with the second PCB. After the tester has been matched against all 21 PCBs, its average score is calculated. Then the next tester is sent through the matching algorithms until all 7 testers have been matched against each PCB. These results are stored and printed out by the Results program.

Results PCB Tester Matchup Report – The fifth program lists each PCB with its reference number, part number, and description, and each tester, its reference number, part number, nomenclature, and vendor name. Details of this report appear in Attachment III, Section B. The Tester Thoroughness Percentage Table gives the scores of the testers for each PCB. Then, tester shortcomings are listed for all PCBs, describing which parameters in each group failed. If all parameters in a group failed, only the group description is given and listed as a CRITICAL shortcoming.

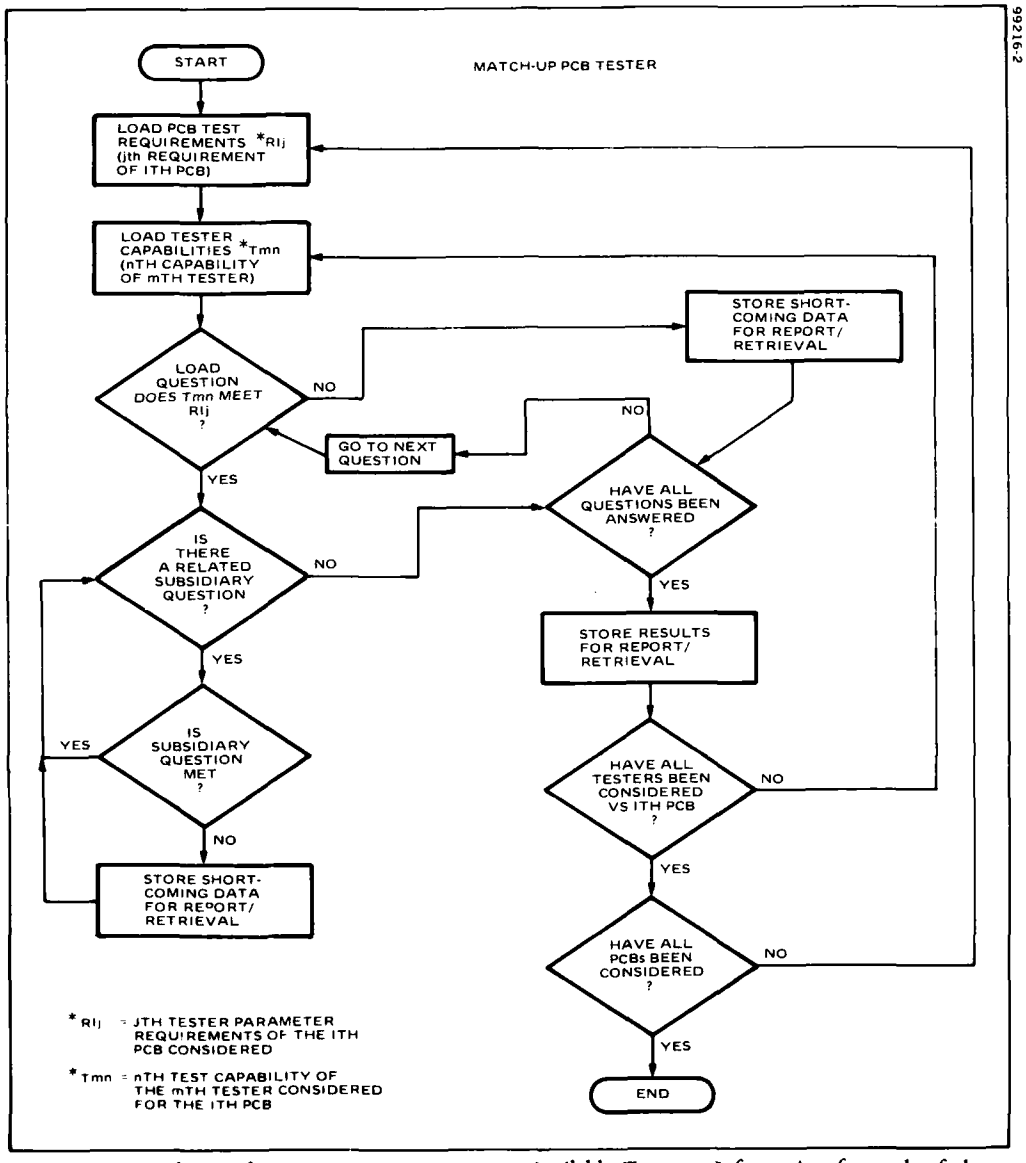
Finally, the Matchup Analysis Summary ranks the testers according to their average thoroughness percentage achieved on all 21 PCBs. This matchup is referred to as the digital parameter compatibility (DPC), which is later combined with other tester factors for the overall composite ranking.

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Figure B. Match-Up of PCB Test Requirements to Available Testers. Information for each of the 7 testers is sent through the matching algorithms for the 21 PCBs.

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2. OVERVIEW OF D/PCB REQUIREMENTS/TESTER CAPABILITY DIGITAL MATCHUP REPORT

Following the correlation of D/PCB test requirements to the capabilities of candidate test systems, stored results are processed by the digital match report, which results in tester thoroughness or achievement by D/PCB and tester rank for the set of D/PCBs.

The digital match report, provided in Attachment III, Section B, ranks 7 test systems by average percent thoroughness, or achievement, on 21 D/PCBs. This tester ranking is for digital parameter compatibility (DPC) with the set of PCBs and is later used with other tester factors to arrive at the composite tester rank.

Based solely on digital parameter compatibility, the match report indicates that the Computer Automation, Capable 4000 test system has the highest rank.

The opposite table represents the 5 leading sections of the digital match report, Attachment III, Section B, which are briefly described as follows.

A participating set of 21 D/PCBs is identified in Section 1, page 1, by reference number, part number, and description.

Section 2, page 2, similarly identifies a participating set of 7 test systems.

Section 3, page 3, PCB to Tester Matchup, is a matrix tabulation of each tester's percent thoroughness, or achievement against each of 21 D/PCBs of the set.

Section 4, page 5, lists tester shortcomings for all PCBs. Within a PCB, the parameter group number, set number, and parameter number causing the tester shortcoming are specified. The tester set number usually refers to the first order set of the tester's equipment (as one or more "sets" of power supplies) experiencing the shortcoming.

Next, the shortcoming significance is specified as CONDITIONAL if an individual parameter of a group failed for the tester. A CRITICAL shortcoming is recorded if all tester parameters in a group failed to meet the PCB's parameter requirements for that group. A value rating is assigned the CONDITIONAL or CRITICAL shortcoming.

The shortcoming description lists the parameter description of the failing parameter in the group for a conditional failure. If all parameters of a group fail, only the group description is given, along with the critical failure.

Section 5, Matchup Analysis Summary, ranks tester thoroughness as an overall average percent achievement by the tester on all 21 D/PCBs of the match set. The test system name and number is also specified.

It is important to understand that the tester matchup rank of digital parameter compatibility is only one of several factors used to arrive at the composite tester rank.

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MATCHUP OF PCB TEST REQUIREMENTS TO TESTER CAPABILITY

Digital Match Report Entries
(See Attachment III, Section B)

Ref. *								Section Title
1/1	PCB Reference Number	PCB Part Number	PCB Description					PCB System Ident
	P0001	1646333	Arithmetic Register					
2/2	Tester Reference Number	Tester Part Number	Tester Nomenclature	Vendor Name				Tester Candidate List
	T0001	L-135	Functional Board Test System	Teradyne				
3/3	Tester Reference Number	PCB Reference Number P001	P002	. . . . .	P0021			PCB to Tester Matchups
	T001	93%	91%		98%			
4/5	PCB Reference Number	Parameter Group Number	PCB Set No.	Parameter Number	TST Set No	Shortcoming Significance	Shortcoming Description	Tester Short-comings
	P0001	64	1	9	1	Conditional	What is the Maximum Size of ROM?	
5	Tester Reference Number	Rank	Tester Thoroughness Percentage	Tester Part Number	Tester Nomenclature	Vendor Name		Matchup Analysis Summary
	T0004	1	97%	4000	Capable	Computer Automation		

*Report Section/Page No.

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3. OVERVIEW OF PERFORMANCE EVALUATION FOR NON-DIGITAL PARAMETRIC FACTORS

Each candidate test system was also evaluated for important characteristics other than digital parametric test capabilities. These additional areas included maintenance and support, hardware, test programming, and software.

The questionnaire data received from the tester manufacturers (excluding the section on digital test features) and the report on the "Selection Guide for Digital Test Program Generation Systems," dated October 1978 for NOSC, were used to evaluate four other important performance evaluation factors for selecting a test system. These important factors are:

- Maintenance and Support
- Hardware
- Test Programming
- Software

To ensure a fair and unbiased evaluation for each tester candidate, a method was developed to determine a figure of merit for each of the four factors. In essence, a common baseline test system criteria (based on the findings from the literature search and the technical opinions from the project team members and the project consultant) was created to conduct a figure of merit tabulation of each factor for all seven tester candidates. The procedure outline is illustrated in Attachment III, Section C, Tables 1 through 5. Every item listed for each factor has been assigned a bias factor that would effectively weigh each item with respect to the maximum figure of merit rating. See the facing table for the performance evaluation tabulated results on all seven primary tester candidates. The top four candidates were chosen as the inputs to the tester composite ranking process (discussed in the next topic).

To gain additional knowledge on the individual test system, each tester manufacturer on the primary candidate list was visited by the project team members. A technical discussion and a test system demonstration were presented by the manufacturer's technical staff personnel. After each technical session, a question and answer period was conducted to ensure the understanding of the overall test system performance. Additional documented information on the test system was usually offered by the manufacturer at the time.

The benefits derived from these visits include the following:

- A better understanding on the test system performance
- Direct evaluation of the test system's strong and weak points
- A study on the user and test system compatibility
- A more direct interface with the manufacturer's technical staff as required for followup technical questions on their test system
- Proposed solutions were offered by the manufacturer on testing capabilities not readily available in the test system.

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TESTER PERFORMANCE EVALUATION SCORES

Evaluation Factor	Candidate System						
	CA 4400	GR 1795	Fluke 3040A	HP DTS-70	Teradyne L-135	TI ATS-960	Trace TL-8
Maintenance and Support	76	91	92	86	88	76	60
Hardware	114	117	119	96	137	109	86
Test Programming	230	234	137	191	220	167	144
Software	222	185	91	262	171	211	146
Total Score	642	627	439	635	616	563	436

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4. COMPOSITE RANKING OF EACH TESTER

The composite ranking of the top four primary test systems was achieved by combining the digital performance compatibility (DPC) ratings with the results of the test programming capability, hardware, maintenance and support, and software evaluations.

The tester composite ranking includes the results from the computer match-up report discussed in Topic 2.C-2 and the results from the evaluation of non-digital parametric factors discussed in the previous Topic, 2.C-3. The composite scoring chart with a weighing factor for each category is shown in Table I of Attachment III, Section C. The top four test system candidates and their respective scores are shown in the facing table.

To summarize the results, Hewlett-Packard leads in the Tester Software and Teradyne in the Maintenance and Support areas. Strong in the area of Tester Hardware is Teradyne and in the area of Digital Performance Compatibility is Computer Automation. To round up the fifth category, GenRad is the leader in the Test Programming capability of the Performance Evaluation as shown in Figure A. At this stage of the Performance Evaluation, Computer Automation is the leading candidate with 836 points and GenRad is second to Computer Automation with 817 points. The four test system candidates overall cumulative scores are shown in Figure B.

A brief discussion of each of the five Test System Performance Evaluation areas of consideration follows.

First, the Digital Performance Compatibility (DPC) ratings were extracted from the matchup analysis summary of the matchup report in Attachment III, Section B. An extensive and comprehensive effort was made to ensure that the Tester's testing capabilities would satisfy the D/PCB test requirements surveyed, including the four MIRADCOM benchmark digital printed circuit boards. From the analysis made on the MIRADCOM cards, there were four hybrids with analog or analog/digital characteristics. Two of these were analog hybrids (P/N 390104 and 390105) and two were analog/digital hybrids (P/N 390011 and 390013). These parts cannot be tested wholly or partially with the present digital test system configuration under evaluation for this project. However, conclusive evidence derived from these analyses demonstrated that all the test systems selected as primary candidates could test most or almost all of the functions of the printed circuit boards surveyed. The tester shortcomings are listed in the Matchup Report (Attachment III, Section B) for every PCB surveyed.

The Test Programming capability of each test system was based on a report submitted to Naval Ocean Systems Center. The report, "Selection Guide for Digital Test Program Generation Systems," dated October 1978, was chosen for this project because of its thoroughness, comprehensiveness, currency, and unbiased evaluation of the existing test program generation systems.

Next, the Test System Hardware features is related to the digital parametric analysis since the features dictates the tester testing capabilities. Number of drivers/sensors, switchable I/O pin, programmable drivers/sensors, and hardware growth potential were among the important features being sought.

The relative ease or degree of difficulty with providing for maintenance and logistics support is an important factor in selecting testers. Therefore, certain elements of maintenance and logistics support were carefully evaluated in the composite ranking process. Elements such as test system reliability and manufacturer's ATE service support, were given prime consideration. In addition, size of the manufacturer, ATE market volume of manufacturer, and number of D/PCB testers sold of the type proposed for procurement, are good historical indicators for the test system under evaluation.

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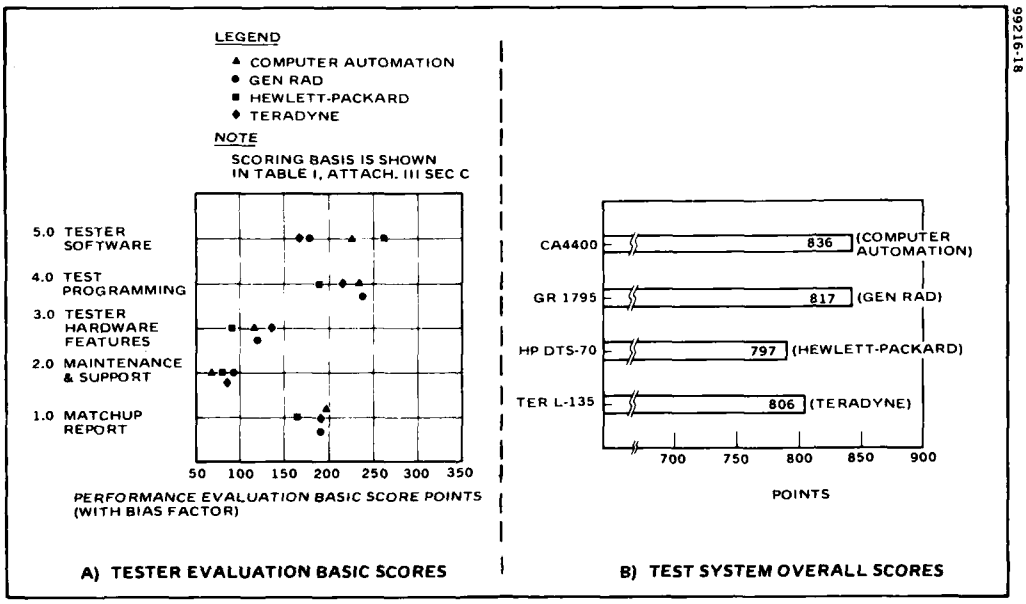
Finally, the tester's background/foreground capability was considered one of the most important items in the Tester Software evaluation. About 40% of the maximum figure of merit rating for tester software was distributed to background/foreground capability.

The raw tabulated data for the four tester candidates are shown in Attachment III.

The composite ranking scores are the major contributions in the Theoretical Test System Selection discussed in Topic 2. F-1.

THE TOP FOUR TEST SYSTEM CANDIDATES COMPOSITE SCORES

Subject \ Candidate	CA-4400	GR-1795	HP DTS-70	Teradyne L-135
Tester Software	222	185	262	171
Test Programming	230	234	191	220
Tester Hardware Features	114	117	96	137
Maintenance and Support	76	91	86	88
Matchup Report (with bias factor)	194	190	162	190
Test System Overall Scores	836	817	797	806



As may be noted, the relative ratings varied for each subject. The overall scores were highly-weighted inputs to the final selection.

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1. RECOMMENDATIONS FOR TESTABILITY IN MILITARY SPECIFICATIONS

The review of the adequacy of testing provisions in military specifications resulted in specific recommendations for development of three documents and updating others. Additional results are a brief summary of known current testability activities by DoD and the military services, and a bibliography of military specifications involving testability.

The military specification review task reported in this subsection consisted of the following three subtasks.

- Provide recommendations for MIL-STD testability specifications.
- Establish a Testability Design Guide.
- Provide specific recommendations to MIRADCOM for improving the testability of four MIRADCOM-supplied PCBs.

Specification Review Task Summary – The list of specifications for review was established from bibliographies, references, and indexes, as limited to military specifications, standards, and handbooks. The original 80 documents identified were culled to 23 of significance to testability, graded by the review into five classes. These classes are specifications with (1) numerous testability references, (2) moderate testability references, (3) slight testability references, (4) minor or indirect testability references, and (5) references to testability solely through pertinent or associated definitions. Details of the document review are presented in Attachment IV A (with associated Appendix) and are summarized below. The review results in a bibliography of military specifications on testability.

Basic Results – The main recommendation involves three documents: (1) a Testability Standard, (2) a Test Program Sets Standard, and (3) a Testability Handbook. The opposite table shows the application matrix of 12 existing specifications that apply to the proposed documents.

Testability Standard – The military standard on testability should set a definition for testability, testability prediction, and testability measurement. For replaceable assemblies, it should establish testability design requirements and prediction and measurement standards. It should also assign engineering responsibilities for its application, and management responsibility for its realization.

Test Program Set Standard – The military standard on Test Program Sets should be directed to establishing the elements needed to test a hardware unit in the light of system maintenance concepts. These elements include test factors among which are BIT/BITE tests, ATE self-test, test program design, and order of testing. Other elements include adapter design factors, test facilities requirements, and test implementation means. The test requirement set should provide means to measure the testability of a unit under test (UUT) to verify the testability prediction and achievement of the required diagnostic resolution.

Testability Handbook – The military handbook on testability should be a specific workbook of various testability design techniques (such as are contained in the Testability Design Guide), procedures for predicting testability, and methods of testability measurement. It should contain ways to achieve the test comprehension needed for a desired level of diagnostic resolution, including measuring the resultant. It should also establish means of implementing requirements imposed by the Testability Standard, and alternate methods of achieving requirements implosed by the standard on Test Program Sets.

Other Documents – Specific recommendations are also made for 17 specifications falling in the first four classes, outlined above, for the testability reviews. The significant points or recommendations are primarily updating and

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referencing the suggested documents. Where appropriate, specific document references are included in the appendix. The fifth review class (pertinent definition) consists of a register of applicable documents.

Testability Activities – To complete the military testability specifications survey, a list of known testability activities by the Department of Defense, and other military and naval services is included.

The purpose is to supply information to MIRADCOM and various military agencies on current Government activity for improving military specifications on testability.

APPLICATION MATRIX OF EXISTING SPECIFICATIONS
TO PROPOSED TESTABILITY DOCUMENTS

Existing Specification Document	Candidate for Consolidation into		
	Testability Standard	Test Program Sets Standard	Testability Handbook
AR-10A (NOTE 1)	Yes (NOTE 1)		
MIL-STD-415D	Yes		
MIL-STD-1326 (NAVY)	Yes		
MIL-STD-2076 (AS)	Yes		
MIL-STD-2077 (AS)		Yes	
MIL-E-11991D (MI)			Yes
MIL-M-24365A (SHIPS)	No	No	No
MIL-STD-1519 (USAF)		Yes	
MIL-HDBK-239 (NAVY)	No		Source
MIL-T-24309 (SHIPS)	Yes	Yes	
MIL-T-28800B	No		
MIL-STD-1378B	Source		

NOTE 1: AR-10A is to be replaced by MIL-STD-2084 (pending).

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2. OVERVIEW OF THE TESTABILITY DESIGN GUIDE

The recommended Testability Design Guide aids the design team in understanding the military user's need for testable digital PCBs. It shows how to meet this need to enable better and more cost effective maintenance in the using military organizations.

The Testability Design Guide is a unique consolidation and summarization of significant rules, practices, suggestions and studies pertinent to the testability of digital PCBs. It is intended as a primary reference for system planners, contractors, managers, and designers. The document is a compilation and condensation of information from interviews, seminars, and approximately 135 articles from the literature. It is divided into eight subtopics plus a comprehensive bibliography, as shown in the table opposite.

The Design Guide first considers the question"What is testability?," the perspective being the entire 1980s decade. Based on authoritative answers, the guide is organized around all major aspects of testability from the general design rules to considerations of basic design, test philosophy and management. Emphasis is placed upon practical rules with freedom of choice to meet differing needs. Most of these subtopics further group rules pertaining to a common functional aspect.

The general purpose ad hoc rules were developed for SSI/MSI logic but also apply to other logic densities and families.

The general rules for large scale devices are those that apply particularly to LSI, VLSI, VVLSI including microprocessors and support chips, ROMs, RAMs, UARTs, etc. They also include rules for busses and memory testing.

The special rules for test points emphasize optimum placement to expose buried nodes, to ease fault testing, or to enable a unique test mode in the logic.

An adapter is the mechanical and electrical interface between test set and the UUT. The rules for design emphasize common features, human engineering, high usage, simple maintenance, software, long life and minimal cost.

Modeling, simulation, and automatic test procedure generation rules consider aspects that enable the most effective use of automatic test equipment. A goal was to illustrate some approaches recommended for modeling LSI/VLSI devices, including microprocessors, and the use of these models in establishing the testability of a design.

Design methods for testability improvement considers some of the approaches discussed in the literature to incorporate significant testability into design at the chip level. Some of these approaches can be used in part at the board level. One goal is to identify some of the tradeoffs required to achieve better testability.

The test philosophy and scenario rules are incorporated to emphasize the global aspects of testability as compared to local PCB aspects. Design for testability must consider both the user's test philosophy and the test scenario pertinent to the employment of the complete system.

Management for testability is concerned with the special problems, tradeoffs, conflicts, and decision that arise from incorporating considerations of testability into the design and fabrication of a system. The goal is to publish this expansion of the manager's role and responsibilities.

The bibliography lists the basic sources for the Testability Design Guide; it also lists some pertinent textbooks. It is organized into fourteen topics, with each paper assigned to a single topic. The object is to provide the source for details, explanations, and additional study, and to acknowledge efforts of those working to further testability in practice.

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HIGHLIGHTS OF THE DESIGN GUIDE

- Organization – the why and the how
- General purpose (ad hoc) testability rules
- General rules for large scale devices
- Special rules for test points
- Adapter rules-mating the tester to the PCB
- Modeling, simulation, and automatic test procedure generation
- Design methods for testability improvement
- Test philosophy and scenario
- Management for testability
- Bibliography – the sources for details, explanations and further study

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3. MIRADCOM PCB TESTABILITY IMPROVEMENTS

Detailed logic circuit examination of the MIRADCOM Digital Autopilot benchmark PCBs yielded 19 specific recommendations in each of the four PCBs. These recommendations increase the average testability 17 percent.

MIRADCOM benchmark PCBs, of four types identified in the opposite table, were examined for initial and improved testability. Detail results of this task appear in Attachment IV, Section C.

In performing the testability improvement task, the following definition of testability was applied:

- Testability – the ability to perform a functional PCB test on all elements (circuit logic or ICs) at the edge connector.

With the existing design, the logic circuit of each PCB was thoroughly analyzed for its testability. The deficiencies were noted and corrective actions were prescribed. For example, in Digital Autopilot No. 1 (390037) one of the six testability conditions analyzed was as follows:

- Condition – Oscillator cannot be disabled or bypassed.
- Action – Use a gate to provide edge connector access.

When the No. 1 PCB was fully analyzed, six recommendations were made and the initial testability was calculated at 75 percent, corresponding to entries in the table. After logic improvements were introduced, the testability was recalculated and the improved value of 90 percent appears in the table. Thus, the No. 1 PCB net testability improvement is 15 percent as shown. The table shows that 19 specific recommendations were made to the four PCBs. Average testability was also improved 17 percent, based on logic circuit control and accessibility.

In Attachment IV, Section C, three general recommendations are stated which apply to testability improvements of all four PCBs. The general testability deficiencies and corrective actions (recommendations) are restated for direct reference.

- Condition – Digital Autopilot PCBs do not apply available test points.
- Action – Apply test points at vital signal, control, I/O, or power lines.
- Condition – Not all intermodule connections are available to the test system.
- Action – Provide edge connector pins for data bus, address bus, and control line interconnections. Alternatively, provide jumpers to permit opening bus and control lines between modules.
- Condition – Logical inputs tied directly to a high logic reference are not accessible for tester control of logic state.
- Action – Except for low power Schottky devices, apply a logic high to element inputs through a pull-up resistor.

Additional specific PCB recommendations to improve testability include the application or use of various logic gates to:

- Control logic high or low state.
- Control or access counter, shift register or loop interconnections.
- Avoid multiple wired AND logic nodes.
- Avoid ICs with internal wired logic and inaccessible nodes.

Results of the testability improvement task indicate that MIRADCOM benchmark PCBs analyzed can significantly increase testability, through stated improvements, to achieve functional test levels of 90 percent or better.

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MIRADCOM, DIGITAL AUTOPILOT BENCHMARK PCB TESTABILITY
RECOMMENDATIONS AND IMPROVEMENTS

PCB Part Number	Type Number	Testability			
		Recommended Actions	Present %	Improved %	Net % Improvement
390037	1	6	75	90	15
390038	2	3	80	92	12
390039	3	5	60	90	30
390040	4	5	42	55*	13

*This PCB contains 60% digital and 40% analog circuitry.

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1. PLAN TO ATTAIN DIGITAL FAULT ISOLATION METHODOLOGY OBJECTIVES

The generation of a test program for any D/PCB requires many different types of data to be gathered, processed, and maintained. Accordingly, a general plan for data management of the required complex test data files including test programs, specifications, procedures, and test results was generated to assist in defining and evaluating the optimum test system.

Data management, though time consuming, can be of great value during the iterative creation of a validated test program. Further, the data must be maintained and controlled for future reference. The plan created and followed to expedite this process is shown in the accompanying flow chart.

First Steps – Management of data for test procedures should begin, when possible, prior to test program generation. All available test specification or test procedure information should be stored in a centralized computer data file for access by the test programmer. The test programmer may then extract any useful data to identify the total test requirements for a D/PCB. At this time, it is useful to run a computer matchup of D/PCB test requirements against the test capabilities of the intended test system. The output will be a report of test system shortcomings that will provide assistance in the design of a test adapter, if required. Test specification/procedure data storage and D/PCB requirements to test system matchup routines should be executed on a centralized computer, not a test system computer, since the memory requirements can be great.

Test Program Development – When the test requirements have been completed, the test programmer should begin test program generation. The type of test system that is to be used greatly affects the amount of time required to generate a test program. The test programmer should have at his disposal the capability to generate as much of the test program off-line as possible, as shown in the attached flowchart. This will assist in the elimination of syntax errors and minimize the impact of test program generation on production testing of other units under test (UUT), when the test system is time-shared between test generation and testing. The portions of a test program that should be generated and edited off-line include the following:

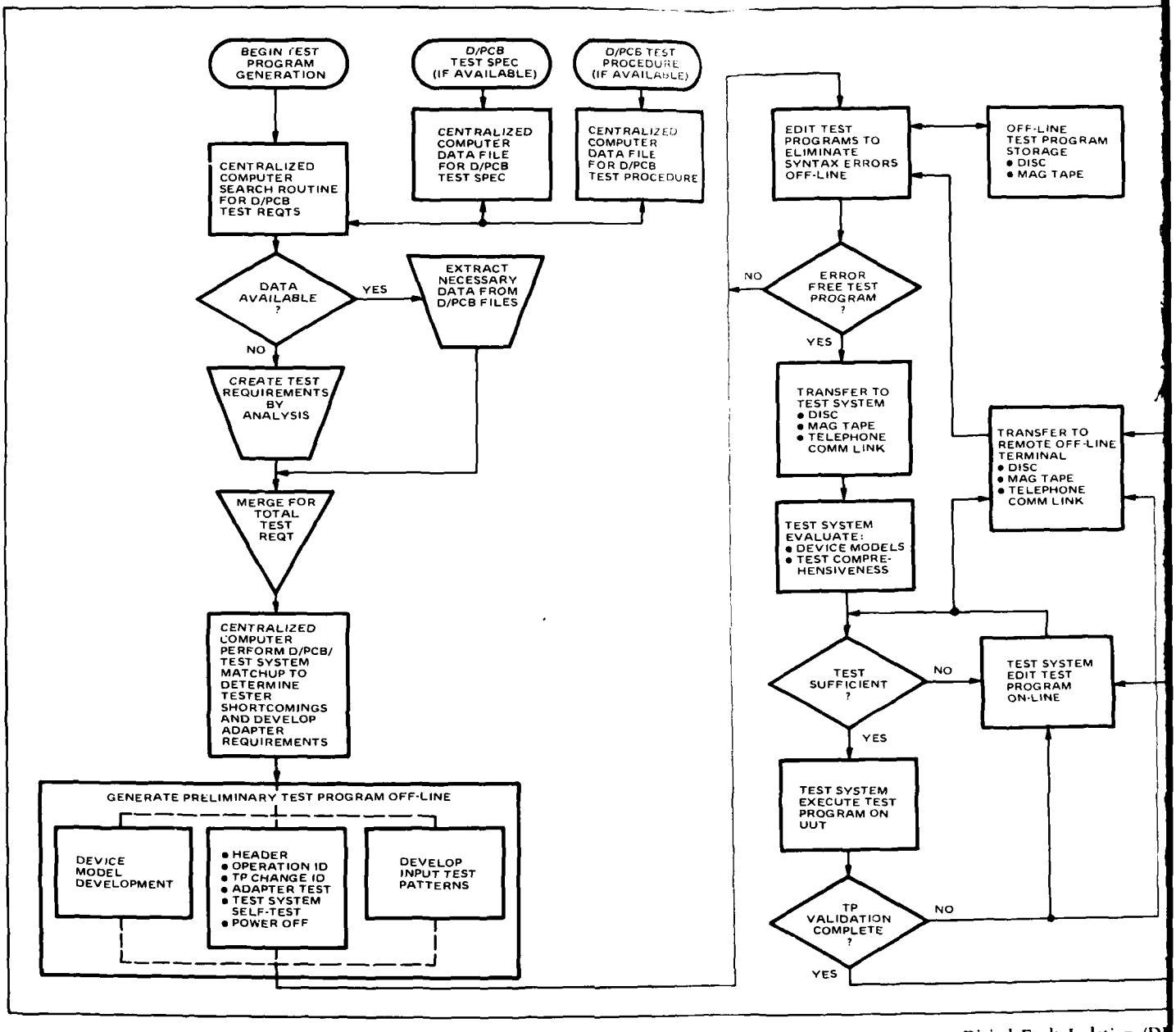
- Header – general format of test program
- Test operation identification structure – method by which authorized operators and correct test programs for a UUT are initialized
- Program revision identification structure – method by which only authorized personnel may alter any test program
- Adapter self-test – test to ensure adapter is functional prior to UUT power-up
- System self-test – test to validate operational capability of the test system
- Device models – generation of the syntax error free operational device models
- Manual guided probing information
- Power down procedures

These tasks are time consuming and if only performed on the test system can reduce the time available for other test system functions. The programmer should have access to this capability from remote terminals located in areas that optimize transfer of information between programmers and data storage facilities. In addition, the test programmer must have the capability to store in-process test programs. This should be accomplished using a storage media which is compatible with the test system in use.

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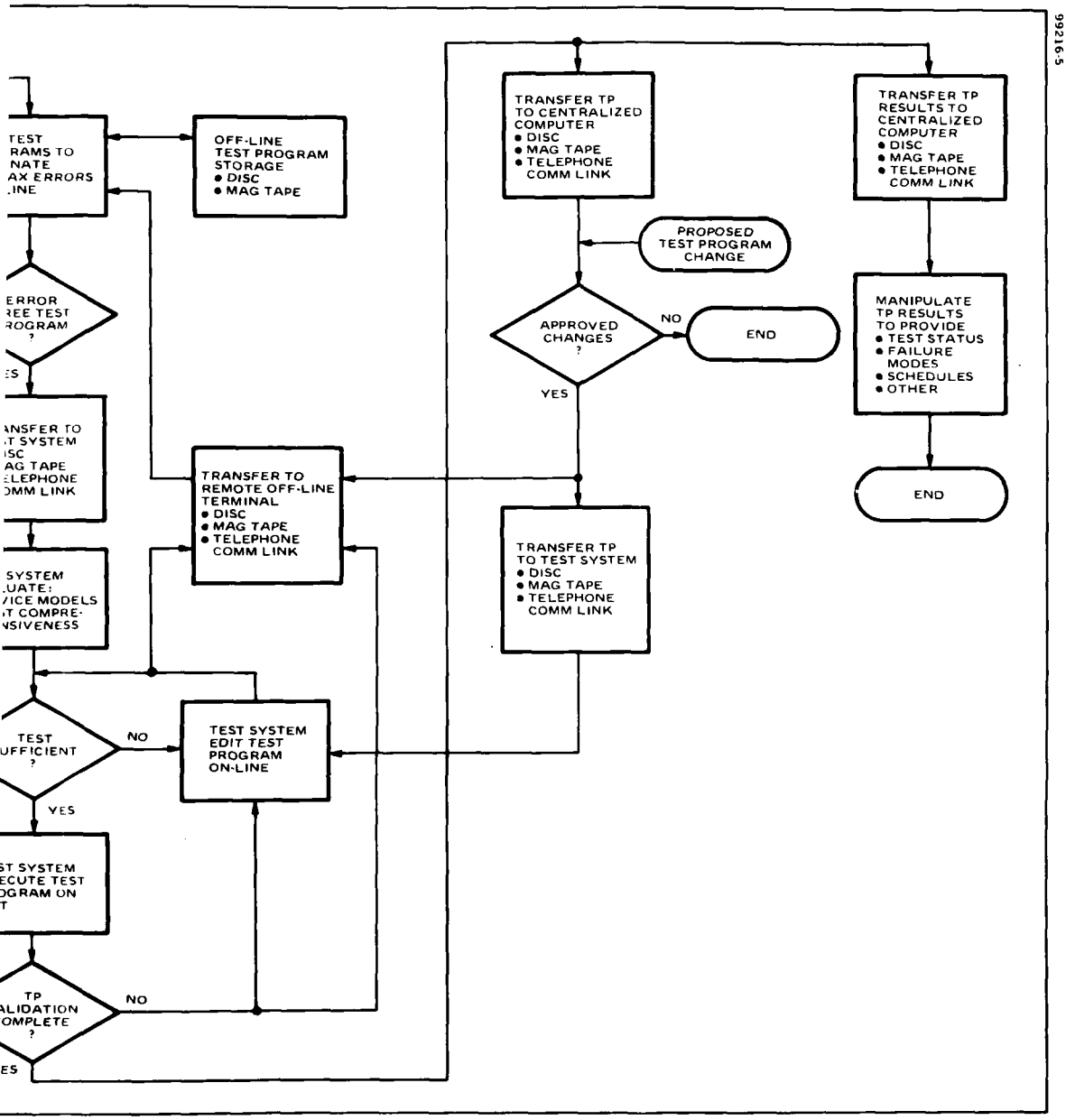
Digital Fault Isolation (DF
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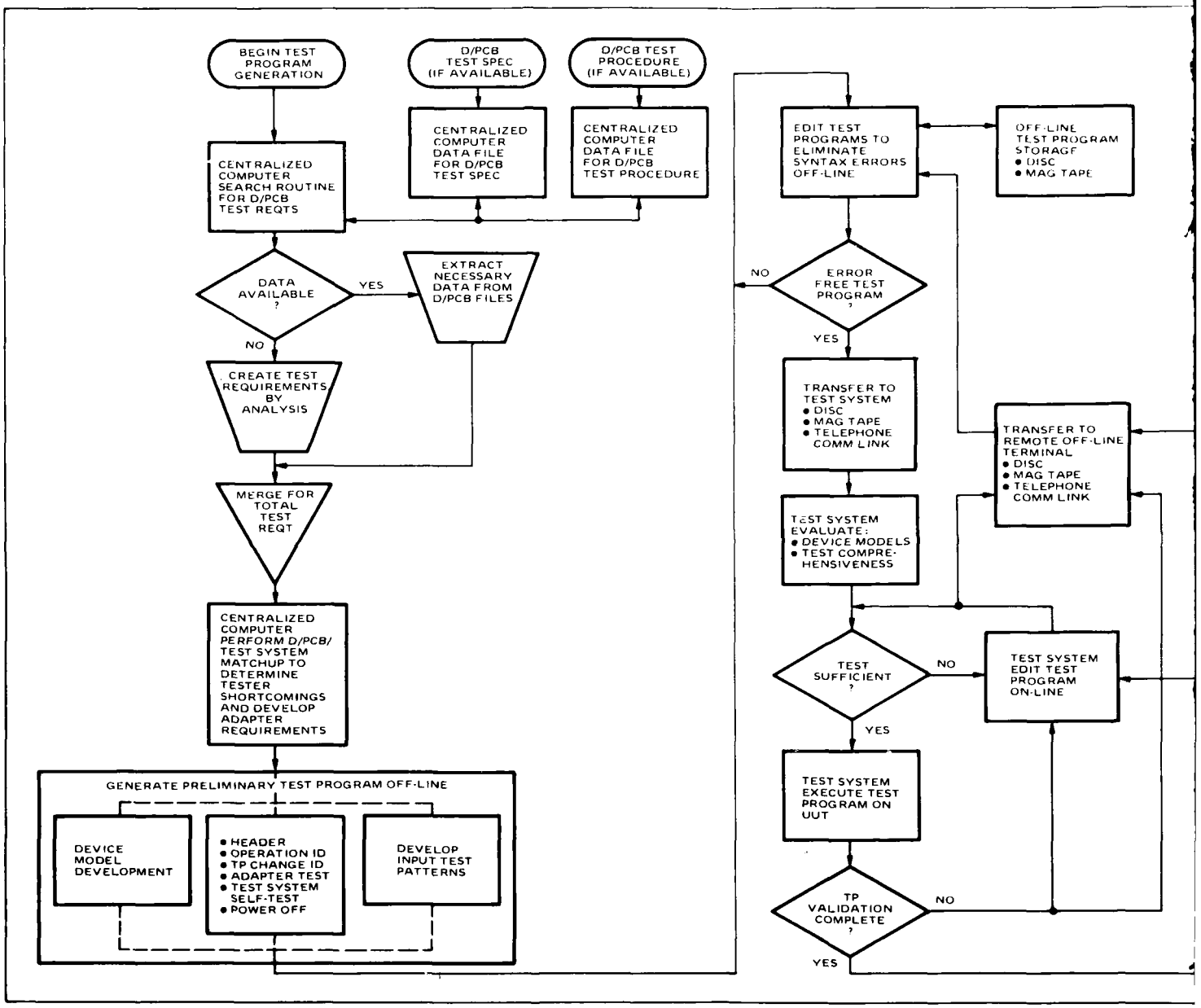


Digital Fault Isolation (DFI) Methodology Objectives. The flow chart shows the general approach to the test program generation and data handling process.

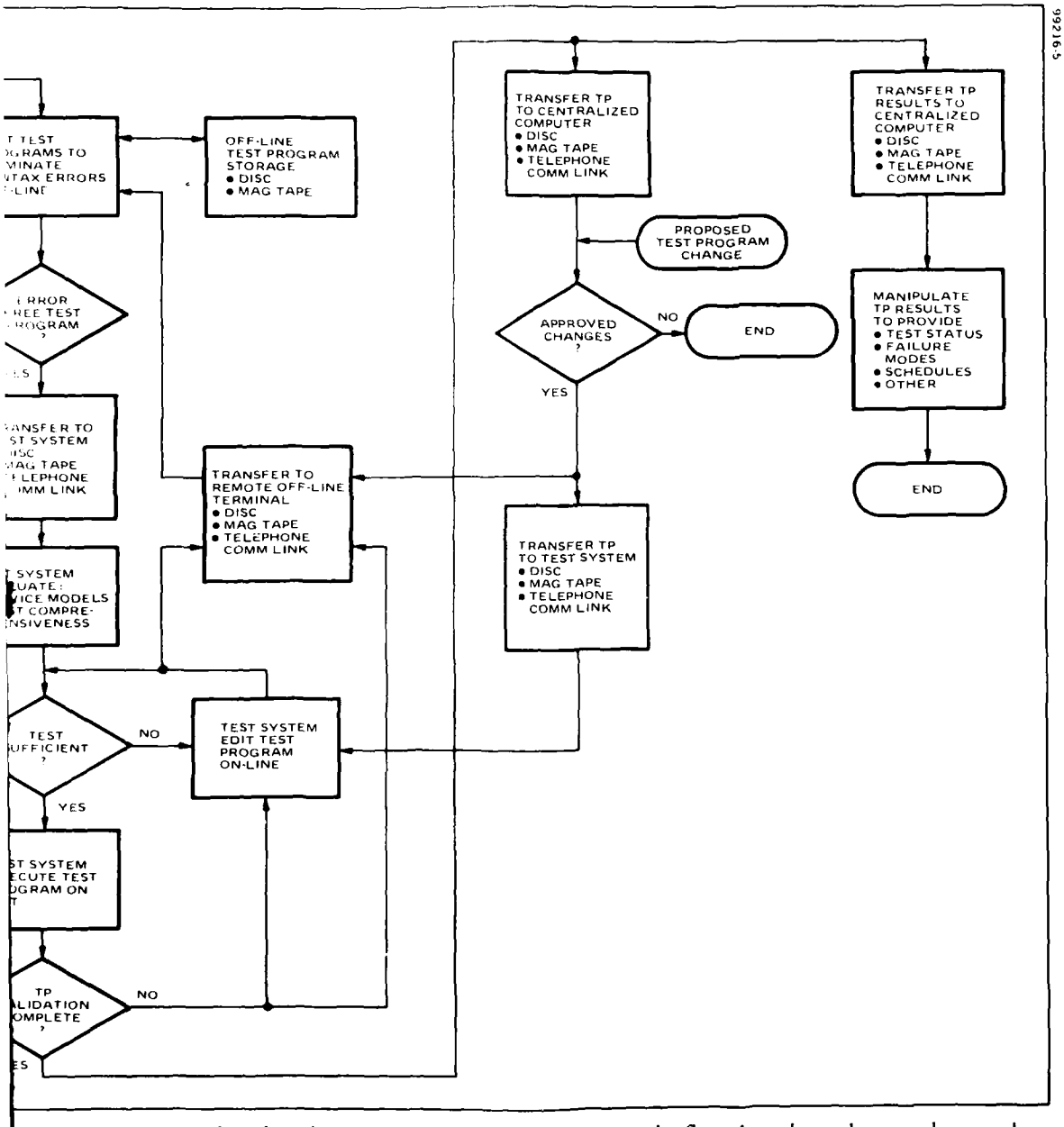
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Digital Fault Isolation (DFI)
the test program generation



Digital Fault Isolation (DFI) Methodology Objectives. The flow chart shows the general approach to the test program generation and data handling process.

Test Program Validation – Once the preliminary programming is complete, the test system must then be used to evaluate the test comprehensiveness of the selected input test patterns. Some test systems have software capable of automatically simulating and generating complete sets of input test patterns as well as evaluating the test comprehensiveness. One advantage of this type of software is that there is no requirement to have any test procedures or specifications to generate test programs that will meet the desired test comprehensiveness level. After the desired level is achieved, the test program may be validated using a UUT and the required adapter.

Validation of the test program will probably be an iterative function since both a "go-chain" test and a fault isolation test must be proved. The "go-chain" test determines only that the UUT will pass or fail the test program. The fault isolation test must be conducted by inserting nondestructive faults into the UUT. The test program and test system must detect and isolate the faults to the desired component level. If at any time during the validation sequence a failure is detected in the test program, the test programmer must have the capability to edit the program to relieve the failure. This should be available either on-line at the test system or off-line at a remote programming terminal.

Production Test – When the validation sequence is completed, the program is ready for production testing. The test program must now be a controlled item to guard against unauthorized test program alterations. This can be done by storing the test programs in protected areas. This could be either hard copy storage or preferably computer storage. Transfer of the test programs to a centralized computer for storage via a combination of telephone communications link, disc, or magnetic tape is the optimum approach.

In addition to test program storage, the resultant test data from test runs must be stored and manipulated to provide production management with high visibility of the entire production test sequence. This data should be used to provide management with test status and failure mode reports. Some test systems provide software packages that provide the desired data base management. Most, however, do not. This capability can be achieved, though, on most test systems which have a computer that can be programmed to do other functions besides test system operation. In most cases, the data base management software is not resident on the test station simultaneously with the test system simulator or operational software. Therefore, to reduce the impact on production testing, data management capability should be executed by an external computer. Transfer of the data should again be performed by a combination of a telephone communications link and disc or magnetic tape transfer.

Impact of Automation – Automated test programs present one additional concern. Changes to test programs can be expensive and therefore must be monitored closely. Some basic ground rules are required to manage this problem. First, it is imperative that the test programming organization be involved in the review cycle of any proposed change. They must evaluate the impact of the change on any existing D/PCB test program. Following change approval by project level management, only authorized personnel may be allowed access to the test program to make the necessary changes. This authorization structure is established in the generation of the initial test program. Also, it is important to establish a means by which the test program can be linked to a D/PCB. In some cases, approved changes are made to a selected group of serialized D/PCBs. In this case there may be more than one test program for a single D/PCB part number. This can be easily accomplished by including a test number of each D/PCB.

Recap – All of the above items combine to make up a very complex system of data management. The test system which can most easily adapt, in whatever form, to these general plans would optimize the production testing of a D/PCB.

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1. TEST SYSTEM THEORETICAL SELECTION

Based on verified supplier data for test system composite rank score, D/PCB test program cost score, and quoted system cost-performance evaluation, the Hewlett Packard DTS-70 achieved a marginally higher potential for DFI application.

Theoretical selection of the Hewlett Packard DTS-70 resulted from further evaluation of verified supplier data, cost effectiveness of D/PCB test program cost, and the quoted system cost-performance.

Results of this evaluation appear in Table I which shows that the DTS-70 total score marginally leads the CA 4400 and GR 1795 test systems.

Result Confirmation – To provide assurance and to confirm the proper system selection, a technical conference was scheduled at each of the four respective supplier's home plants to verify test system data received by Hughes.

In addition, to assist in arriving at the final system selection for DFI, each supplier fully cooperated in conducting a practical performance test of their system. Through mutual effort by the supplier, Hughes, and Dr. L. P. Henckels (consultant for DFI) the test examined two vital system functions: (1) simulator software, and (2) test diagnostics or fault isolation. The next topic (2F-2) discusses results of the test and final system selection.

Composite Score – The composite score achieved by the four final candidate test systems appearing in Table I consists of two parts: the digital parameter matchup and the non-digital test system factors previously discussed and verified.

To each system composite score was added the relative D/PCB test program score, and the evaluated cost-performance score derived from the test system specification (Attachment II, Section C), and the received price quotations (Attachment III, Section D).

Since a multitude of test system hardware, software, and support factors make it up, the composite score was given a dominant weight of 70 percent for the theoretical system selection as shown in Table I.

Test Program – Relative system D/PCB test program cost was based on a D/PCB of 50 ICs, with 95 percent test comprehensiveness, and fault detection to the IC pin. Details of the D/PCB test program costs appear in Attachment III D-5 Table 4.0 DFI Test System Relative D/PCB Test Program Costs.

A recent Hughes study (Firefinder TMDE/TRA; CERCOM DAAB07-76-C-0893, August 1978) established that the preceding D/PCB test program, using D4 LASAR for the Teradyne L-135 test system, required the equivalent of 6.08 hours per IC. The CA 4400, GR 1795, and HP DTS-70, by comparison require 4.48 hours per IC. Thus the nature of D4 LASAR and the need for a leased external network computer places the Teradyne 50 IC test program cost a factor of 1.36 times higher than any of the other three systems.

Referring to a recent simulator report (NOSC; N00123-78-C-0333, October 1978), a test program standard of 3 Hr/IC was used to develop the respective system D/PCB test program point score. The standard-to-actual Hr/IC ratio, expressed as a percentage, was further multiplied by a 3.51 bias factor to achieve the 20 percent total system score weighting. Test program calculations appear in Table II for the respective entries in Table I. System D/PCB test program scores retain the relative 1.36 times factor mentioned above by which the Teradyne L-135 received less points.

Cost-Performance – Test system cost-performance scores in Table I account for a weight of approximately 10 percent of the total system score.

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TABLE I. THEORETICAL SELECTION OF THE DFI TEST SYSTEM

Item	Weight %	Test System Score Achievement			
		CA 4400	GR 1795	HP DTS-70	Teradyne L-135
Composite Rank (Digital-Non Digital)	70	836	817	797	806
Relative D/PCB Test Program	20	235	235	235	173
System Point Rating (Cost/Performance)	10	83	97	136	70
TOTAL POINTS		1154	1149	1168	1049

TABLE II. RELATIVE D/PCB TEST PROGRAM COST POINT RATING

Item	Test System Achievement			
	Unit	Teradyne L-135	Other (1)	Standard (2)
D/PCB Test Program	Hr/IC	6.08	4.48	3
Point Rating	—	173	235	—

$$\text{Point Rating} = \frac{\text{Standard Hr/IC}}{\text{System HR/IC}} \times 100 \times \text{Bias Factor}$$

CA, GR, HP $\quad PR = \frac{3}{4.48} \times 100 \times 3.5 = 235$

Teradyne $\quad PR = \frac{3}{6.08} \times 100 \times 3.5 = 173$

Bias Factor = 3.51 used to weight D/PCB test program point score to 20% of total system score in Table I.

Estimate Conditions:

D/PCB	50 ICs SSI, MSI
Test	95% Comprehensiveness
Fault Isolation	IC pin level

(1) CA 4400, GR 1795, HP DTS-70
(2) NOSC; N00123-78-C-0333, October 1978

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1. TEST SYSTEM THEORETICAL SELECTION (Continued)

Cost Adjustments and Specification Points – A thorough evaluation of each test system price quotation was performed by assigning a standard point rating to each item of the system specification in Attachment II, Section C.

Because of inadequacies or variations existing in the system price quotations for the complement of UUT power supplies required by the specification, it was necessary to make normalizing adjustments in hardware and price to each system quotation. Thus UUT power supplies were equalized as much as possible in all test systems.

Other items such as IEEE-488-Bus and software options were included and scored accordingly. Attachment III, Section D-1 provides a detailed tabulation of adjusted price and specification points accumulated by each test system quotation, under the heading "DFI Test System Quote Evaluation."

A summary of the resulting system price (Attachment III, Section D) and specification scores from Attachment III, Section D-1 appears in the first and second row of Table III.

The test system specification point scoring method allows each system quotation to seek its own score level independent of observer subjectivity.

Cost-Performance Ratio – As a measure of test system cost effectiveness, a cost-performance ratio was defined. This ratio takes the test system price and divides it by the specification point score achieved. The lowest test system cost-performance ratio, therefore, identifies the highest value system.

In Table III the DFI standard test system has an objective price of $145,000 and a specification point score of 589, for a cost-performance ratio of 246. Similar figures appear in Table III for the four test system quotations showing adjusted system price, specification point score, and quoted cost-performance ratio achieved.

The test system point score, in the bottom row of Table III, is the ratio of the objective cost-performance to the quoted cost-performance expressed as a percentage. Since the DTS-70 test system achieved the lowest cost-performance ratio, it gained the highest point score of 136 as shown. The test system point scores discussed are applied in Table I to determine the theoretical system selection.

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TABLE III. DFI TEST SYSTEM COST-PERFORMANCE POINT RATING

	Standard System Objective	Quoted System Achievement			
		CA 4400	GR 1795	HP DTS-70	Teradyne L-135
System Price	$145,000	$163,948	$132,907	$124,284	$195,002
System Specification Point Score	589	556	523	687	555
Objective Cost/Performance	246	---	---	---	---
Quoted Cost/Performance	---	295	254	181	351
Point Rating	100	83	97	136	70

$$\text{Cost-Performance} = \frac{\text{System Cost \$}}{\text{Specification Point Score}}$$

$$\text{Point Rating} = \frac{\text{Objective Cost/Performance}}{\text{Quoted Cost/Performance}} \times 100$$

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2. FINAL TEST SYSTEM SELECTION – THEORETICAL AND PRACTICAL SCORING

Through a combined theoretical evaluation score and a practical performance test score of the test system simulator and fault diagnostic capability, the study selected the Hewlett-Packard DTS-70 test system for DFI application.

Selection of the DTS-70 test system resulted from a total score of 1514 points, achieved through an evaluation of theoretical and actual performance.

Overview – Final evaluation of the four test systems (shown in Table I) included two major parts: (1) Theoretical Evaluation, and (2) an experimental System Performance Test. The theoretical evaluation consists of the verified point score discussed in Topic 2.F-1. The system performance test was devised to provide actual measured system data concerning two system functions: (1) Simulator Software, and (2) Test Diagnostic or fault isolation. Through the combined theoretical and systems performance test results, a substantive system evaluation and selection was attained.

Practical Evaluation – Simulator software performance and fault diagnostic capability of all four test systems was measured by a test circuit having 5 ICs. The test circuit, logic diagrams, and test program for this test were supplied by Dr. L. P. Henckels. For ready reference, details of the test circuit measured results, and test evaluation determined by Dr. Henckels are included (unabridged) in Attachment III, Section F.

By devising a test circuit with relatively few ICs, the resulting test program for the test system experimental session was of mangeable length (70 to 80 steps). However, the test circuit contained difficult logic test conditions to stress the test system simulator software and fault diagnostics, or isolation capability. In this, a set of 5 predetermined test circuit fault conditions were presented to each test system to determine its fault isolation performance.

Explanation of Data Evaluation – The performance test result scores as determined by Dr. Henckels' evaluation appear in Attachment III, Section F, Figure 3. The shaded scores in Figure 3, however, were not used in the systems measured achievement score appearing in Table II of this topic, as noted below. To illustrate the derivation of the measured achievement score in Table II, the CA4400 system is used as an example.

In Figure 3 (Attachment III, Section F) the CA4400 "Simulation Scores" are: (9) + (10) + 9 = 28. The value of 28 divided by 36 (rating) and multiplied by 100 equals the 78 score in Table II for the "Simulator Software" of the CA4400. In other words 28 x 100/36 = 78 is the CA4400 Simulator Software score used for further evaluation.

Similarly from Figure 3 the CA4400 "Testing Score" is: (7) + 3 = 10. Since the maximum score value is 16 the "Test Diagnostic" score in Table II of this topic is: 10 x 100/16 = 63 as shown for the CA4400 system. The other system scores were developed along similar lines for the values in Table II.

Where appropriate, the use of a number with parenthesis, (N), was used from Figure 3. These numbers are an extrapolation of the measured value (without parenthesis) and represent a studied assessment of the system's optimum capability.

Again, (with reference to Figure 3) the Testing Score for "Pin Diagnostics" was not used, to maintain normalized system hardware throughout the DFI evaluation. This is because at least one other system, besides Gen Rad and Teradyne, has a logic pin analyzer probe available, but it was not used in the test. Furthermore, all systems were previously scored in the theoretical system evaluation for the IC pin isolation probe.

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Also, (irrespective of operator training, experience, or intellectual ability) the System Score, "Ease of Use" in Figure 3 was not used in the final system evaluation. The reason is that this category covers system features relating to human factors and thus deals with subjective matters. In addition, and since time would not permit, this score is the result of a single observation event and thus not a true extended statistical sample.

TABLE I. FINAL THEORETICAL AND PERFORMANCE SELECTION OF THE DFI TEST SYSTEM

Item	Approx Weight %	Test System Score Achievement			
		CA 4400	GR 1795	HP DTS-70	Teradyne
Theoretical Evaluation					
Verified Score[1]	75	1154	1149	1168	1049
System Performance Test					
Simulator Software	13	179	179	186	0 (205)
Test Diagnostics	12	160	160	160	255
Total Score		1493	1488	1514	1304 (1509)

Simulator Score = Simulator points x 2.3
(factor of 2.3 is used to achieve approximately 13% weighting)

Diagnostic Score = Diagnostic points x 2.55
(factor of 2.55 is used to achieve approximately 12% weighting)

[1]Digital – Non-Digital, D/PCB Test Program, Cost/Performance – Composite Score

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2. FINAL TEST SYSTEM SELECTION – THEORETICAL AND PRACTICAL SCORING (Continued)

Performance Measurement – The system measured aghievement scores in Table II used in the final evaluation (supplied by the cited Figure 3) are summarized as follows.

- Simulations Software
  - Accuracy of circuit model,
  - Time to simulate, and
  - Work around required for test circuit.
- Diagnostics
  - Accuracy of fault location to a circuit node, and
  - Number of probes required to isolate a fault (or time).

Results – System performance test scores recorded in Table II were combined with the theoretical system score in Table I. Since the theoretical score contains the bulk of system study data, it was assigned a dominant weight of approximately 75 percent as shown in Table I. Accordingly, the system performance test accounts for the balance of 25 percent weight, distributed 13 percent to simulator software and 12 percent to test diagnostics.

To achieve the distributed weighting, the simulator score of Table II was multiplied by a weighting factor of 2.3. Similarly, the test diagnostics score weighting factor used is 2.55.

It is apparent from Table I that the system performance test score elevates the DTS-70 system to a total high score of 1514 points and thereby selects the DFI recommended system.

The second ranked system is the CA4400 with a total score of 1493, while the GR1795 ranks third with 1488 points.

System performance scores in Table I for the Teradyne L-135 system require clarification to provide a normalized ranking with other systems.

Discussion of the Teradyne L-135 – Since it relies on an external leased VAX system simulator, the L-135 is in a different generic test system class from the other three. The L-135, therefore, cannot be compared directly for the simulator software performance because the three other systems use a self-contained simulator. Although the L-135 simulator software achieved a score of 205 as shown in parenthesis, a value of zero was entered in the final score because of the non-resident simulator feature.

In test diagnostics, the L-135 was by far the best performer. Since this portion of the performance test is directly attributable to the L-135 system, it was scored at full value.

The L-135 total normalized score is therefore 1304 which ranks it fourth against the first three systems. If the simulator software score is included, the total score is 1509 as shown in parenthesis. While the L-135 system performance test score (205 + 255) is the highest achieved, by its nature the L-135 system does not satisfy the DFI program requirements. Its chief disadvantages are high initial or acquisition cost, and high D/PCB test program or test software cost. System performance is otherwise excellent, being fastest in circuit simulation and fault location, with high capability in accuracy of fault isolation to an IC pin.

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TABLE II. TEST SYSTEM SIMULATOR AND FAULT DIAGNOSTIC MEASURED PERFORMANCE[1]

Item	Approx. Weight %	Test System Measured Achievement			
		CA 4400	GR 1795	HP DTS-70	Teradyne L-135
Simulator Software	55	78	78	81	89
Test Diagnostics	45	63	63	63	100

Notes: Simulator Points = Measured achievement x 100/36
Diagnostic Points = Measured achievement x 100/16

[1]System Simulator and Fault Diagnostic relative performance measured with 5 IC test circuit by Dr. L.P. Henckels. Refer to Attachment III, Section F for circuit details, data, and results of Figure 3.

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1. SELECTED TEST SYSTEM DATA BASE MANAGEMENT

Each test system was evaluated based on the capabilities defined for the DFI Methodology. The Hewlett-Packard DTS-70 test system provided the most extensive on-line data base management software.

The major objectives set by the "Plan to Attain Digital Fault Isolation (DFI) Methodology Objectives" are best met by the Hewlett-Packard DTS-70 Test System with Image 1000 Data Base Management Software.

These objectives include:

- The ability to store and manipulate data files that contain test programs, specifications, procedures and test results.
- Accessibility of the Data files by the test programmer.
- Short term storage capability during test program development.
- Test comprehensiveness which is an evaluation program to determine how well the test program is testing a PCB (i.e., percent fault detection).
- The ability to perform program modification and editing on-line. This enables the test programmer to correct any program faults that develop during program execution or generation. Considerable programming time can be saved by having immediate fault correction capability.
- The protection of data files from unauthorized modification.
- Provide management with accurate information of the production test sequence. With this information management will be readily able to identify chronic problems that may develop in the test procedures or in the PCB design-manufacture process. This enables management to achieve maximum efficiency and throughput.
- The ability to modify and update existing data files in addition to the creation of new files.

Also, with the addition of optional memory, the Hewlett-Packard DTS-70 test system could be programmed to provide a matchup of PCB requirements and test system capabilities that would generate a list of tester shortcomings. This parameter-by-parameter comparison and correlation, similar to the one performed by Hughes during the DFI basic effort, can provide an indication of how well a test system can test a PCB as well as providing necessary adapter design information. If performed manually, this information is time consuming and costly.

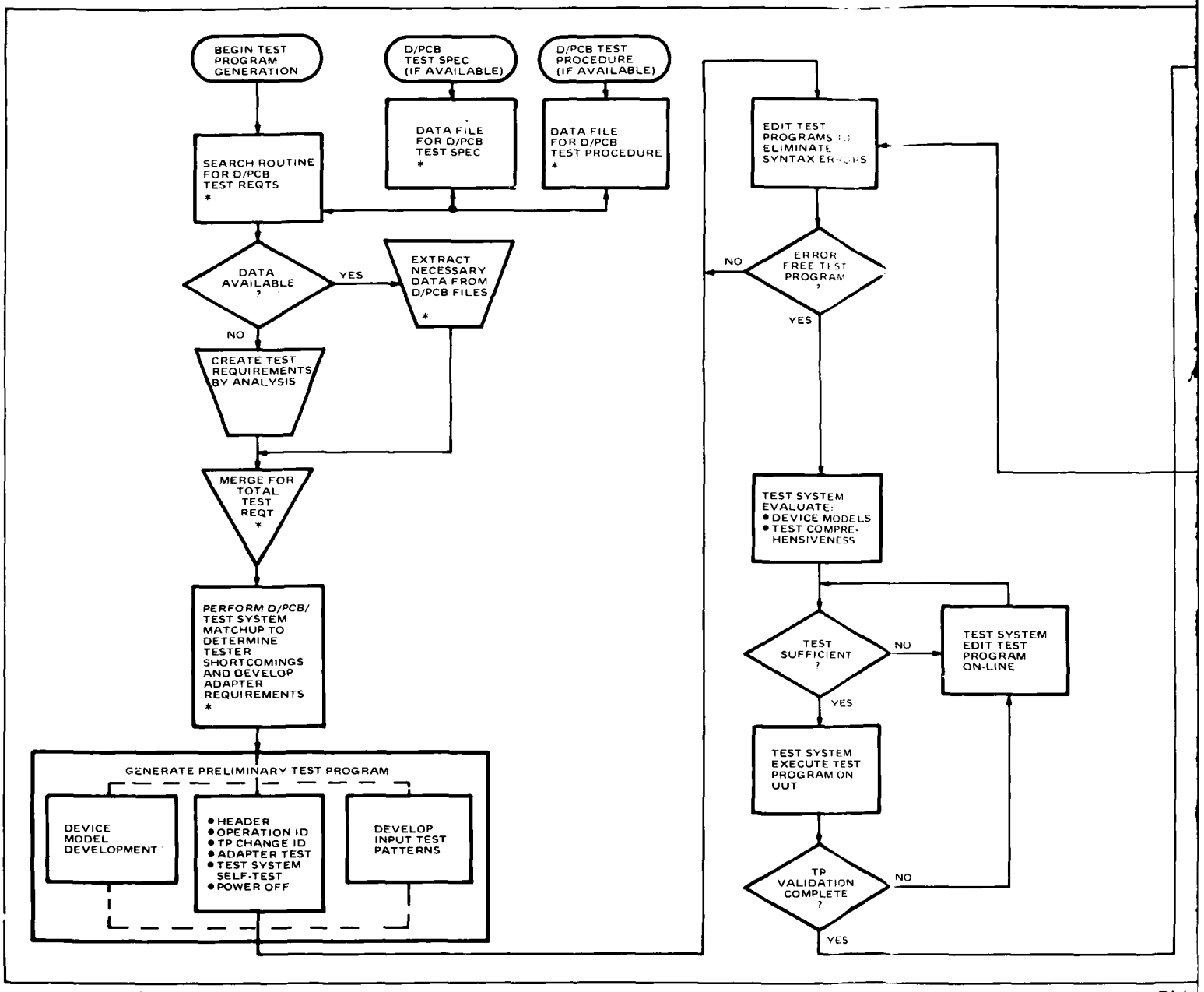
Of all the test systems evaluated, the Hewlett-Packard DTS-70 test system with IMAGE 1000 software best satisfied the objectives for DFI Methodology. Use of the DTS-70 System would optimize the production testing of the PCBs by reducing the man-hours required and increasing the throughput. The accompanying flow chart illustrates the process of data base management on the Hewlett-Packard system.

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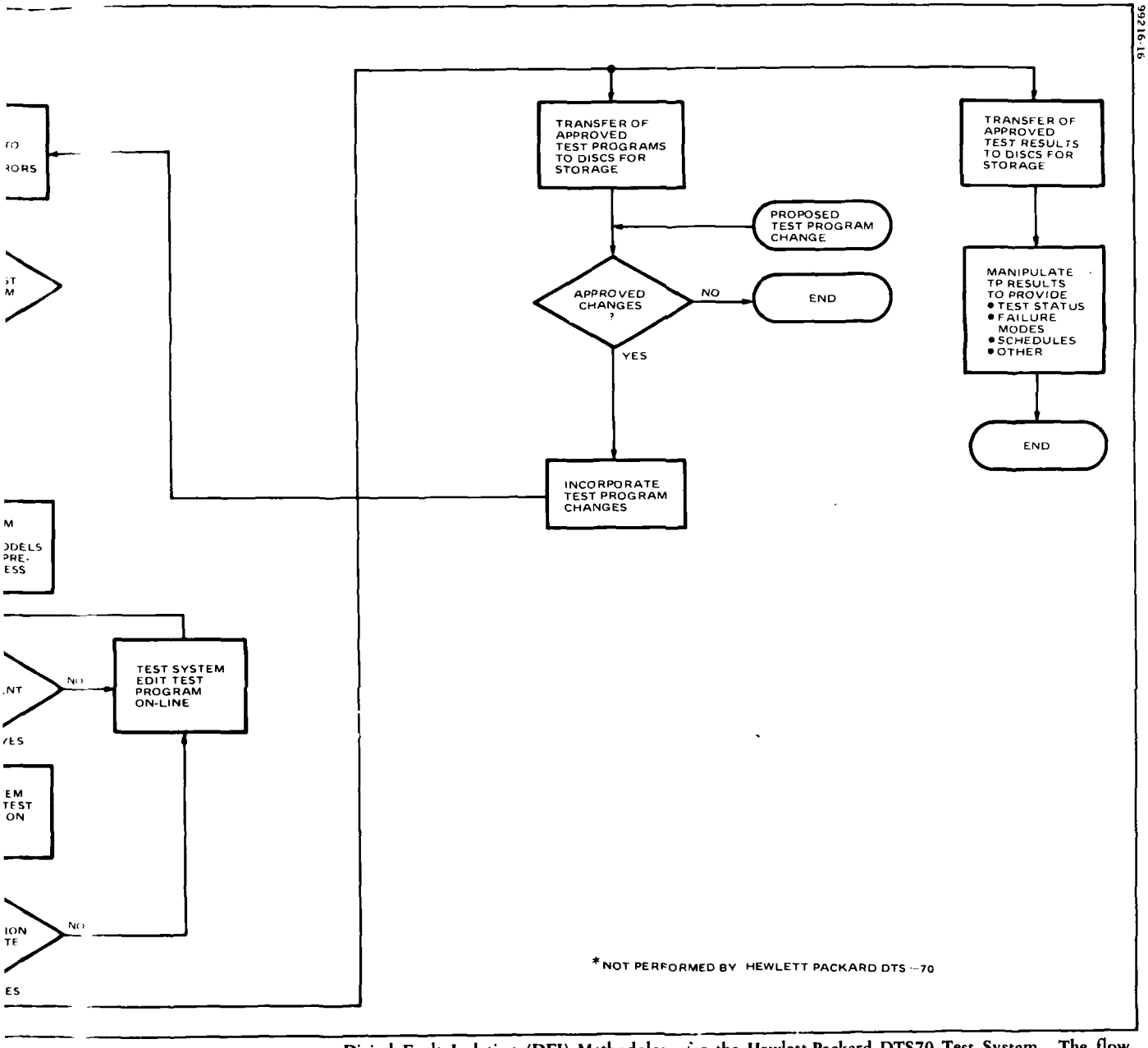


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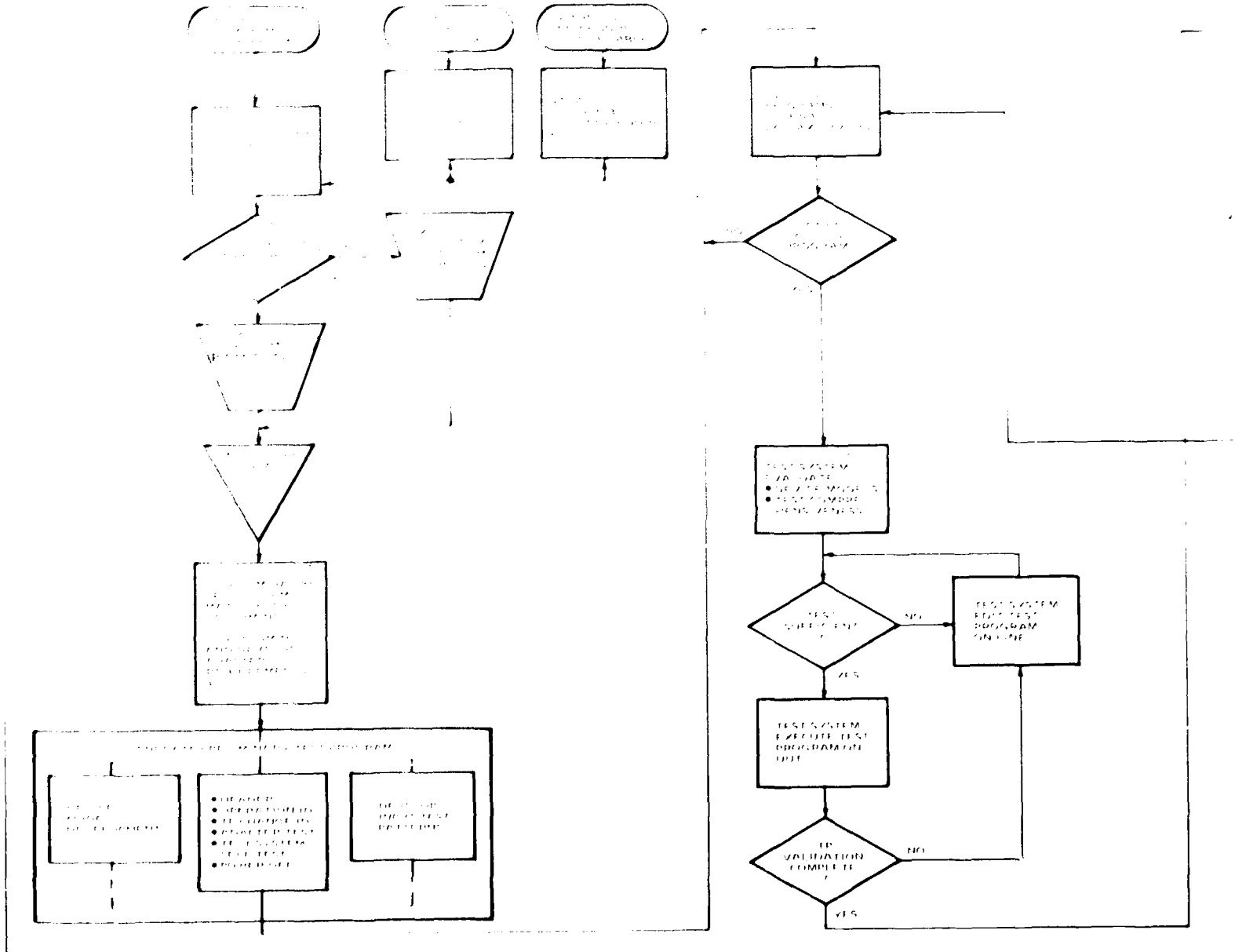
Digital Fault Isolation (DFI) Methodology for the Hewlett-Packard DTS70 Test System. The flow chart shows the approach to the test program generation and data handling process.

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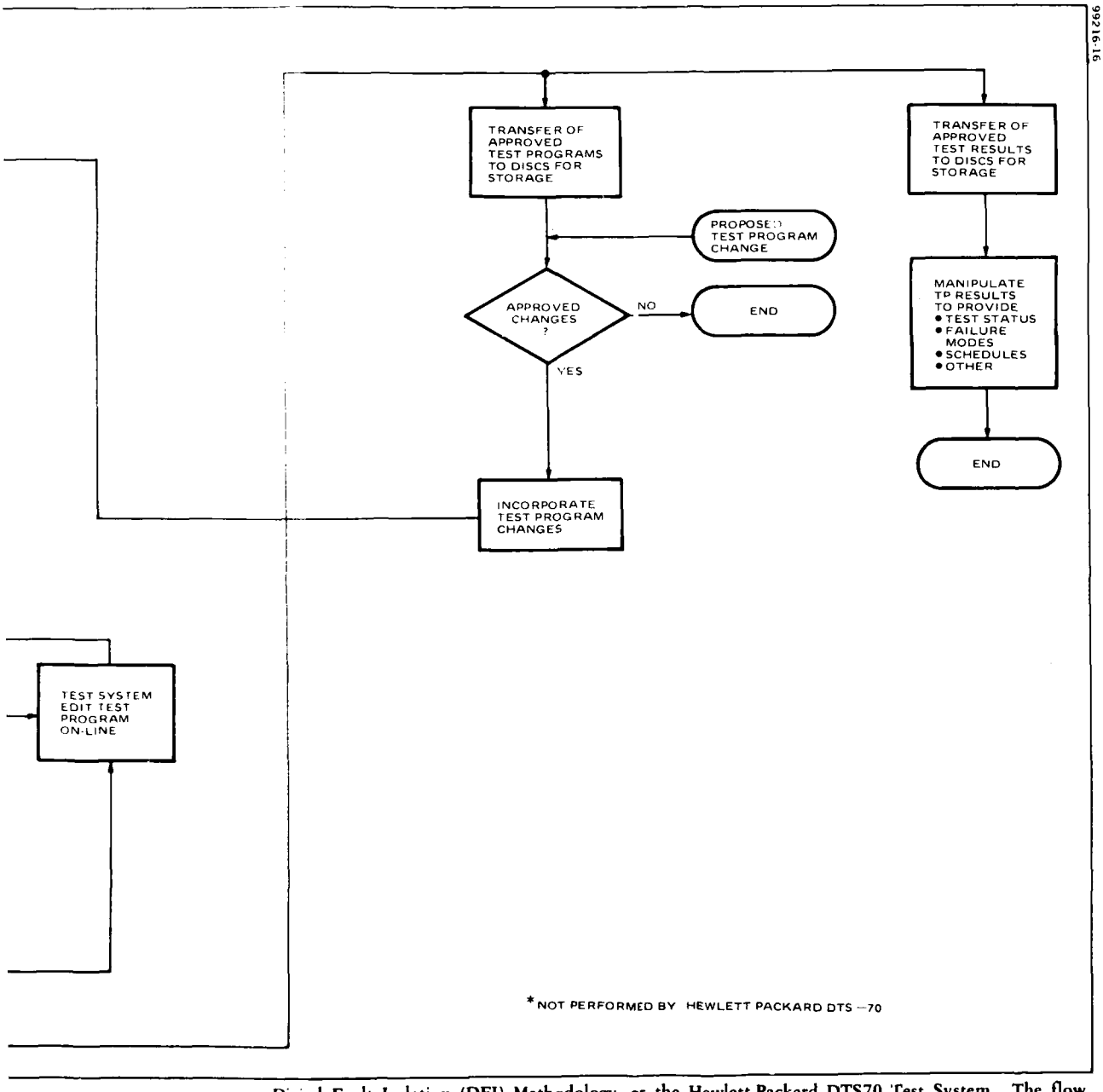
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Digital
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Digital Fault Isolation (DFI) Methodology or the Hewlett-Packard DTS70 Test System. The flow chart shows the approach to the test program generation and data handling process.

SECTION 3
DETAILED DESCRIPTION OF THE SELECTED TEST SYSTEM

1. Digital Printed Circuit Board Test Features and Production Test Capabilities 3-0

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1. DIGITAL PRINTED CIRCUIT BOARD TEST FEATURES AND PRODUCTION TEST CAPABILITIES

Numerous characteristics and capabilities of the Hewlett-Packard DTS-70 system make it efficient and effective in the testing of digital printed circuit boards.

The Hewlett Packard DTS-70 System is comprised of both software and hardware. The software includes the TESTAID III, FASTRACE, IMAGE 1000 data base management, and the controlling RTE IV Real Time Executive. The DTS-70 hardware is capable of expanding to support 6 time sharing terminals in various combinations such as 3 test terminals, 2 remote programming terminals, and 1 data base management terminal. The software packages and hardware combined with the 2113A computer w/256 K memory, 7906A 20 M byte disc drives, 2608A 400 LPM line printer, 2645 CRT terminals, and foot switch attachments, form an efficient test system that meets the requirements specified in the Digital Printed Circuit Board test system specification dated 21 May 1979. The accompanying block diagram illustrates the DTS-70 test system hardware configuration.

Software - TESTAID III is a computer based logic simulator that models the functions of the logic circuit boards. The input to the TESTAID III program comes from the circuit schematic and the parts list. The input phase is achieved by entering the circuit schematic information into the system in a descriptive computer language. The actual components are obtained from a model library which contains models of over 1500 devices. After circuit modeling the TESTAID III simulator begins the task of generating test patterns to completely test the PCB for faults. Manual patterns may also be used, if necessary, and combined with the computer generated patterns to form an adequate test set. The ability to insert manual test patterns enables the test programmer to exploit any prior knowledge he may have of the PCB. For example, entering a grey code pattern to test a grey code counter.

The simulator takes the test pattern set, both manual and computer generated, and applies it to the PCB model. The simulator determines the output of the circuit model, good and faulty, for every input pattern. When the output pattern differs from the output pattern of a known good model, faults are identified. These fault signatures (fault output response patterns) are stored for latter use by the FASTRACE software in fault diagnosis. The software also gives the programmer knowledge of the overall test pattern effectiveness and test quality in terms of percent fault detection.

If the PCB fails the GO/NO GO tests (faulty output response patterns are detected during the TESTAID III analysis) the system goes into the FASTRACE fault isolation mode. FASTRACE directs the operator to probe the appropriate locations on the PCB to isolate the fault. The combination of a fault signature search from the TESTAID III files and input from the guided probe enable rapid and accurate trouble shooting of the PCB to the component or IC level.

Digital Controller - The Digital Test Unit portion of the DTS-70 includes the electronics that provide the output pattern to the PCB (driver function) and that detect the output responses (receiver function). With the options selected, the DTS-70 system will have the following characteristics:

- 270 programmable driver/comparators.
- Driver/comparator threshold levels programmable between + 16v to - 16v. This enables testing of PCBs containing more than one family of logic, i.e., TTL and CMOS.
- Programmable rate generator capable of generating pulses at a rate of 5M bits/sec. This enables the rapid clocking of such devices as shift registers and counters.

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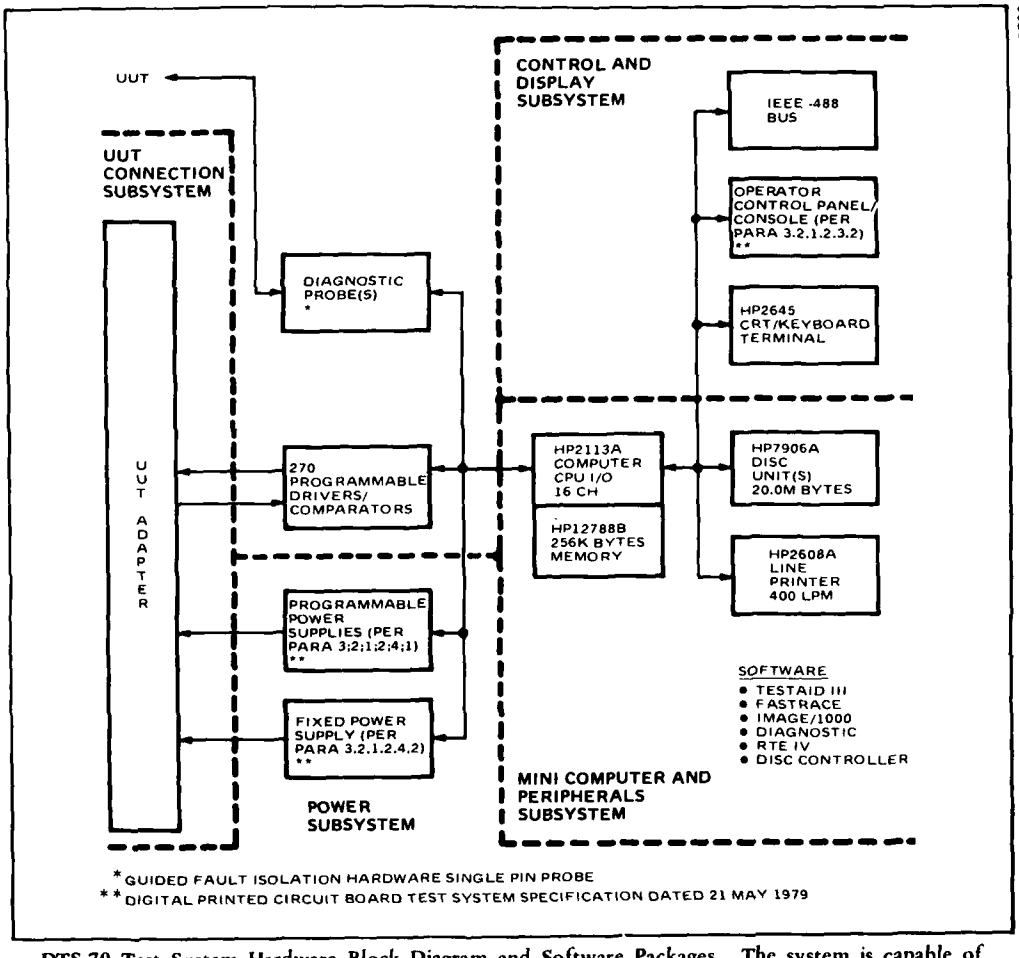
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Use or disclosure of proposal data is subject to the restriction on the Title page of this Proposal.

- IEEE 488 bus which enables the use of bus-programmable equipment in conjunction with the test station for analysis of analog or hybrid PCBs.

The DTS-70 software and hardware forms an efficient test system that meets the requirements of the Hughes Digital Printed Circuit Board Test System Specification dated 21 May 1979.



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DTS-70 Test System Hardware Block Diagram and Software Packages. The system is capable of expansion to support 6 time sharing terminals.

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SECTION 4
RECOMMENDATIONS, CONCLUSIONS, AND ACKNOWLEDGMENTS

1. Recommendations 4-0
2. Conclusions 4-1
3. Acknowledgments 4-2

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Section 4 – Recommendations, Conclusions, and Acknowledgments

1. RECOMMENDATIONS

Recommendations for further actions involve (1) broadcast of the optimized testability design requirements that were identified during the study, and (2) assurance that the schedule for the MIARADCOM demonstration of the selected test system to industry is realistic.

Prior to completion of the DFI basic effort, several items were identified which merit further action or study. The pertinent recommendations, summarized in the table below, are as follows.

Testability – Promote and coordinate development of unified Army, Navy, and Airforce Testability Standards under the aegis of Industry Joint Services, Automatic Test Conference board members. Specific Military standards recommended to be formulated include:

- Testability Standard,
- Test Program Sets Standard,
- Testability Handbook, and
- ATE/UUT Interface Standard (new for DFI).

As appropriate, use separate, generic standards to cover unique requirements of any military service branch.

A preliminary navy testability standard has excellent content – system to PCB – to form a major part of the above DFI proposed Testability Standard. (Reference: "A Study of Testability Standardization for Electronic Systems and Equipment." NESC/NSWC -- Dahlgren, Virginia.)

Test Methods, Requirements – Various methods used to facilitate testing of D/PCBs having LSI and/or microprocessor elements have been identified. The techniques include the following:

- Partitioning
  - -Power, data busses
  - -Logic function
  - -Logic family
- Signature Analysis - SA annotated schematic
- D/PCB Sockets
  - -Removable LSI
  - -Removable microprocessor
  - -Separate LSI, uP component test.
- Use of standard LSIs where possible in place of custom designs
- Use of LSI or microprocessor having testability or self-test features
- Use of LSI with functionally simulated model of external pin level logic transfer states.

In those less numerous cases where a dynamic test must be performed on a D/PCB:

- The test system should have additional provisions to allow testing at full data rates.
- Alternately, the interface fixture or test adapter with high speed capability and IEEE-488 bus control should be used to extend and enhance test system capability.

SUMMARY OF RECOMMENDATIONS

- Promulgate military specifications that will disseminate standard testability criteria
- Formulate, in the military documents, design techniques that enhance testability
- Reflect test hardware lead time requirements in the MIRADCOM industry demonstration schedules

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2. CONCLUSIONS

The following noteworthy conclusions (pertaining to the sample 21 D/PCBs and the 7 candidate test systems evaluated) emerge from the basic effort study results.

1. All seven candidate test systems, computer based or comparison type, have high test capability as determined by the digital parameter match (compatibility) report.
2. Progressive test system screening of digital and non-digital factors for composite rank eliminated two comparison and one simulator type candidate systems from further consideration because of lower scores than the remaining four systems.
3. Screening the test systems for the cost effectiveness of their D/PCB test program (recurring) and their cost-performance (non-recurring) significantly affects system rank and selection by:
   - Enhancing the score of an efficient, high-return-value system.
   - Enlarging the low score differential of a less efficient and low return value system.
4. Automatic test program generation within the test system is presently more cost effective, direct, and desirable for production testing than a leased network computer system.
5. Beyond a theoretical evalution, test systems performance, measured by a practical test circuit, provides substantive assurance in test systems selection.
6. The test circuit of Attachment III, Section F, used to measure test system performance, is useful in providing quantitative speed or time of the system simulator software and fault diagnostics (location).

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3. ACKNOWLEDGMENTS

Hughes wishes to extend due recognition for the professional and cooperative efforts supplied by personnel of all test system companies that participated in the DFI study program.

Special appreciation is expressed for the companies and personnel that graciously offered their services and facilities, gratis, for the system performance tests:

Computer Automation – Irvine, California
General Radio – Concord, Massachusetts
Hewlett Packard – Loveland, Colorado
Teradyne – Boston, Massachusetts

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DIGITAL PRINTED CIRCUIT BOARD SURVEY –

ATTACHMENT I TO INTERIM REPORT (BASIC EFFORT)

MANUFACTURING METHODS AND TECHNOLOGY FOR 'DIGITAL FAULT ISOLATION FOR PRINTED CIRCUIT BOARDS'

PROJECT NO. R783242

CONTRACT DAAK40-78-C-0290
25 AUGUST 1979
CDRL A003

DIGITAL PRINTED CIRCUIT BOARD SURVEY

ATTACHMENT I

TO INTERIM REPORT (BASIC EFFORT)

Manufacturing Methods and Technology for

'Digital Fault Isolation for Printed Circuit Boards'

Project No. R783242

Prepared for

U.S. Army Missile Research and Development Command

Redstone Arsenal, Alabama 35809

Project Officer: G. Little
DRDMI-EAT
(205)- 876-3848

Contract No. DAAK 40-78-C-0290
CDRL A003

Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

Report Date: 25 August 1979
FR79-12-669

SECTION IB
DIGITAL PCB TEST REQUIREMENTS SUMMARY

FOREWORD

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards contraining complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the development of digital fault isolation methodology, and the identification of the corresponding optimum available automatic test hardware.

The subsequent contract option phase of this project involves the purchase, setup, and demonstration of the selected fault isolation hardware/software system, using the developed techniques.

CONTENTS

SECTION IA – DIGITAL PCB QUESTIONNAIRE
SECTION IB – DIGITAL PCB TEST REQUIREMENTS SUMMARY

SECTION IA
DIGITAL PCB QUESTIONNAIRE

```
M     M  IIIIIII  RRRRRR    AAAAA   DDDDDD    CCCCC    OOOOO   M     M
MM   MM     I     R     R  A     A  D     D  C     C  O     O  MM   MM
M M M M     I     R     R  A     A  D     D  C        O     O  M M M M
M  M  M     I     RRRRRR   AAAAAAA  D     D  C        O     O  M  M  M
M     M     I     R   R    A     A  D     D  C        O     O  M     M
M     M     I     R    R   A     A  D     D  C     C  O     O  M     M
M     M  IIIIIII  R     R  A     A  DDDDDD    CCCCC    OOOOO   M     M
```

= MISSILE RESEARCH AND DEVELOPMENT COMMAND =

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

*** DIGITAL PCB QUESTIONNAIRE ***

MANUFACTURER: _____

COMPLETED BY: _____

TELEPHONE NO: _____

DATE: ___/___/___

GENERATION DATE: AUG 21,1979



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	_____
(2).	PCB PART NUMBER (12 CHARACTERS)	_____
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	_____
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	_____
(5).	PCB SYSTEM NAME (16 CHARACTERS)	_____
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	_____
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	_____
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	_____

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?						
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS						
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS						
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)						
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)						
(5).	TTL						
(6).	CTL						
(7).	RTL						
(8).	DTL						
(9).	IIL						
(10).	ECL						
(11).	DCTL						
(12).	RCTL						
(13).	HNIL						
(14).	CMOS						
(15).	NMOS						
(16).	PMOS						
(17).	EIA						
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC						
(19).	OTHER						
(20).	NUMBER OF SSI						

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(21).	NUMBER OF MSI						
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE						
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE						
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)						
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)						
(26).	PCB COMPLEXITY FACTOR						
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)						
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)						
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)						
(30).	TOTAL NUMBER OF IC'S ON PCB						

PARAMETER GROUP: P59 (DIGITAL CHARACTERISTICS - CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAPACITANCE						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)						
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	____	____	____	____	____	____
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	____	____	____	____	____	____
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	____	____	____	____	____	____
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	____	____	____	____	____	____

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	____	____	____	____	____	____
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	____	____	____	____	____	____
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	____	____	____	____	____	____
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	____	____	____	____	____	____

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P62 (DIGITAL CHARACTERISTICS - ONE-SHOTS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DOES PCB HAVE ONE-SHOT DEVICES? (NO=1,YES=2)						
(2).	IF YES, CAN ONE-SHOT(S) BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..						
(3).	EDGE TRIGGERED? (POSITIVE=1,NEGATIVE=2)						
(4).	WHAT IS THE DELAY (PULSE WIDTH) OF THE ONE-SHOTS? DELAY MINIMUM						
(5).	DELAY MAXIMUM						

PAPAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)						
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)						
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)						
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)						
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)						
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)						
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..						
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)						
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)						
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)						
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..						
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)						
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)						
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?						
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED						
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)						
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)						
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?						
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED						
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)						
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)						
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

** * * DIGITAL PCB QUESTIONNAIRE * * **

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)						
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)						
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)						
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)						
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)						
(5).	PIA						
(6).	ACIA						
(7).	PLA						
(8).	UART						
(9).	SAT						
(10).	SAR						
(11).	OTHER						
(12).	OTHER						
	INFORMATION ON SUPPORT CHIPS:						
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)						
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS						
(14).	CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE MICROPROCESSOR? (NO=1,YES=2)						
(15).	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF EACH OTHER? (NO=1,YES=2)						
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

INFORMATION ON THE MICROPROCESSORS:

(17). QUANTITY ..... _____ _____ _____ _____ _____ _____

(18). DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) .. _____ _____ _____ _____ _____ _____

(19). IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) _____ _____ _____ _____ _____ _____

(20). CAN CONTROL LINES ON MICROPPOCESSOR BE DISABLED FROM TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..... _____ _____ _____ _____ _____ _____

(21). MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2; ROM ..... _____ _____ _____ _____ _____ _____

(22). STATIC RAM ..... _____ _____ _____ _____ _____ _____

(23). DYNAMIC RAM ..... _____ _____ _____ _____ _____ _____

(24). CAN MICROPPOCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2) ..... _____ _____ _____ _____ _____ _____

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1). DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)						
(2). DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..						
(3). DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)						
(4). DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)						
(5). DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)						

STIMULUS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	POLARITIES/VOLTAGE(S)						
(2).	ACCURACY						
(3).	MAXIMUM CURRENT DRAIN						
(4).	RIPPLE PEAK TO PEAK						

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)						
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM						
(3).	CLOCK RATE MAXIMUM						
(4).	PULSE WIDTH						
(5).	RISE TIME						
(6).	FALL TIME						
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(8).	HOW MANY OF THIS SET ARE REQUIRED?						
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED						
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

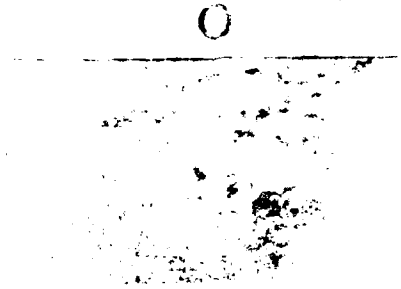
* * * DIGITAL PCB QUESTIONNAIRE * * *

(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)						
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)						
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?						
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?						

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	LOGIC LEVEL "1" MAXIMUM						
(2).	LOGIC LEVEL "1" MINIMUM						
(3).	LOGIC LEVEL "0" MAXIMUM						
(4).	LOGIC LEVEL "0" MINIMUM						
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P71 (DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DATA BIT RATE						
(2).	WORD LENGTH						
(3).	SEQUENCE LENGTH						
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?						
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)						

IF YES, PLEASE ANSWER P72 GROUP

PARAMETER GROUP: P72 (DIGITAL CHARACTERISTICS - SERIAL SYNCHRONIZATION)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6

NOTE: P72 WILL BE MATCHED TO T69 IN THE DIGITAL TESTER QUESTIONNAIRE.

(1).	PULSE REPETITION FREQUENCY						
(2).	RISE TIME						
(3).	FALL TIME						
(4).	WIDTH						
(5).	AMPLITUDE						



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1). WORD RATE						
(2). WORD LENGTH						
(3). WORD SEQUENCE LENGTH						
(4). IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(5). HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?						
(6). IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)						

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P74 (DIGITAL CHARACTERISTICS - PARALLEL SYNCHRONIZATION)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
NOTE: P74 WILL BE MATCHED TO T69 IN THE DIGITAL TESTER QUESTIONNAIRE.						
(1). PULSE REPETITION FREQUENCY						
(2). RISE TIME						
(3). FALL TIME						
(4). WIDTH						
(5). AMPLITUDE						

MEASUREMENTS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB QUESTIONNAIRE * * *

NOTE: THERE IS NO P75 GROUP. THE TESTER PARAMETERS IN P75 WILL BE MATCHED TO P78 AND P80.

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	LOGIC LEVEL "1" MAXIMUM						
(2).	LOGIC LEVEL "1" MINIMUM						
(3).	LOGIC LEVEL "0" MAXIMUM						
(4).	LOGIC LEVEL "0" MINIMUM						
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)						
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?						

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DATA BIT RATE						
(2).	WORD LENGTH						
(3).	SEQUENCE LENGTH						
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)						
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?						
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)						

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB QUESTIONNAIRE * * *

IF YES, PLEASE ANSWER P78 GROUP

PARAMETER GROUP: P78 (DIGITAL CHARACTERISTICS - SERIAL SYNCHRONIZATION)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
NOTE: P78 WILL BE MATCHED TO T75 IN THE DIGITAL TESTER QUESTIONNAIRE.						
(1). PULSE REPETITION FREQUENCY	_____	_____	_____	_____	_____	_____
(2). RISE TIME	_____	_____	_____	_____	_____	_____
(3). FALL TIME	_____	_____	_____	_____	_____	_____
(4). WIDTH	_____	_____	_____	_____	_____	_____
(5). AMPLITUDE	_____	_____	_____	_____	_____	_____

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1). WORD RATE	_____	_____	_____	_____	_____	_____
(2). WORD LENGTH	_____	_____	_____	_____	_____	_____
(3). WORD SEQUENCE LENGTH	_____	_____	_____	_____	_____	_____
(4). IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	_____	_____	_____	_____	_____	_____
(5). HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	_____	_____	_____	_____	_____	_____
(6). IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	_____	_____	_____	_____	_____	_____

IF YES, PLEASE ANSWER P80 GROUP

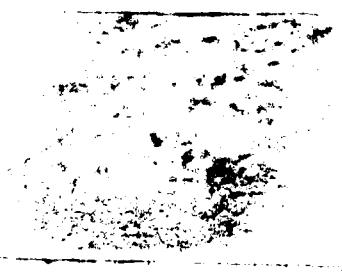


PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB QUESTIONNAIRE * * *

PARAMETER GROUP: P80 (DIGITAL CHARACTERISTICS - PARALLEL SYNCHRONIZATION)

DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
NOTE: P80 WILL BE MATCHED TO T75 IN THE DIGITAL TESTER QUESTIONNAIRE.						
(1). PULSE REPETITION FREQUENCY	____	____	____	____	____	____
(2). RISE TIME	____	____	____	____	____	____
(3). FALL TIME	____	____	____	____	____	____
(4). WIDTH	____	____	____	____	____	____
(5). AMPLITUDE	____	____	____	____	____	____



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MMMMMMM  IIIIIII  RRRRRR    AAAAA   DDDDDD    CCCCC    OOOOO   M     M
MM   MM     I     R     R  A     A  D     D  C     C  O     O  MM   MM
M M M M     I     R     R  A     A  D     D  C        O     O  M M M M
M  M  M     I     RRRRRR   AAAAAAA  D     D  C        O     O  M  M  M
M     M     I     R   R    A     A  D     D  C        O     O  M     M
M     M     I     R    R   A     A  D     D  C     C  O     O  M     M
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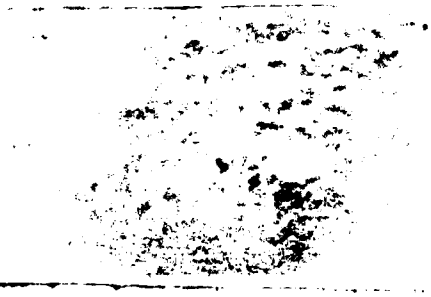
= MISSILE RESEARCH AND DEVELOPMENT COMMAND =

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

DIGITAL PCB TEST REQUIREMENTS SUMMARY

(TABULATION BY PCB)

AUG 21,1979



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	ARITHMATIC REGISTER
(2).	PCB PART NUMBER (12 CHARACTERS)	1646333
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT COMPANY
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/UYQ-21
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	COMPUTER DISPLAY SET
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.910000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.670000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.290000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.220000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.170000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.400000E+01
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.430000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

DESCRIPTION	SET # 1
NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) (1). DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.300000E+01
(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, (2). CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) (3). DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, (4). CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

DESCRIPTION	SET # 1
(1). DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(NO=1,YES=2) (2). DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3). DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

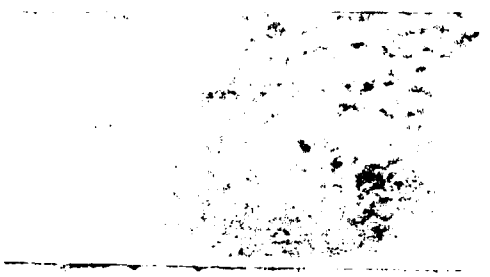
(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.300000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.409600E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)	0.200000E+01
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)	0.200000E+01
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)	0.0
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)	0.934460E+05
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)	
(5).	PIA	0.0
(6).	ACIA	0.0
(7).	PLA	0.0
(8).	UART	0.0
(9).	SAT	0.0
(10).	SAR	0.0
(11).	OTHER	0.0
(12).	OTHER	0.0



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	INFORMATION ON SUPPORT CHIPS:	
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS	
	CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE	
(14).	MICROPROCESSOR? (NO=1,YES=2)	0.0
	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF	
(15).	EACH OTHER? (NO=1,YES=2)	0.0
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)	0.100000E+01
	INFORMATION ON THE MICROPROCESSORS:	
(17).	QUANTITY	0.400000E+01
	DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST	
(18).	POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
	IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM	
(19).	TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
	CAN CONTROL LINES ON MICROPROCESSOR BE DISABLED FROM TEST POINTS	
(20).	OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
	MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2)	
(21).	ROM	0.200000E+01
(22).	STATIC RAM	0.200000E+01
(23).	DYNAMIC RAM	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(24).	CAN MICROPROCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.275000E+01
(4).	RIPPLE PEAK TO PEAK	0.100000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.120000E+08
(4).	PULSE WIDTH	0.300000E-07
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.400000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.400000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

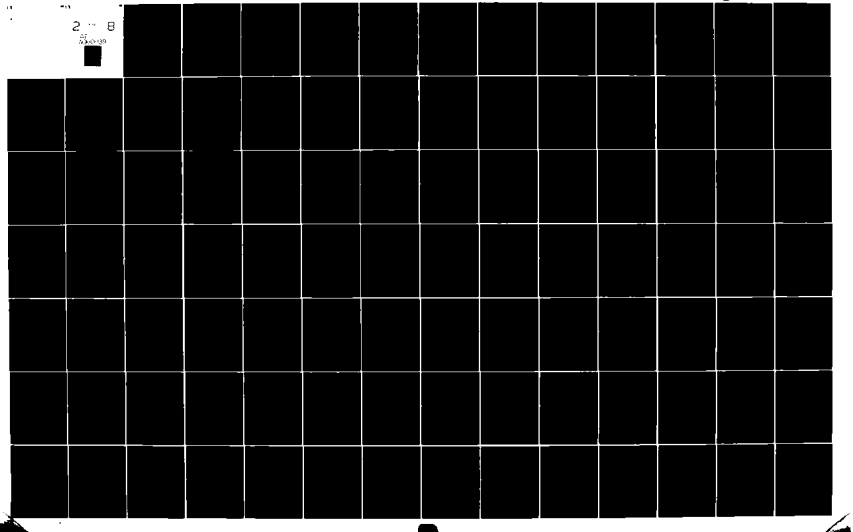
	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.120000E+08

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	-.100000E+00
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

AD-A080 839 HUGHES AIRCRAFT CO FULLERTON CA GROUND SYSTEMS GROUP F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
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P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.500000E+00
(3).	LOGIC LEVEL "0" MAXIMUM	0.240000E+01
(4).	LOGIC LEVEL "0" MINIMUM	-.100000E+00
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.0
(2).	WORD LENGTH	0.400000E+01
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P78 GROUP

PAPAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1
IF YES, PLEASE ANSWER P80 GROUP	

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	MICRO CONTROLLER
(2).	PCB PART NUMBER (12 CHARACTERS)	1640302
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT COMPANY
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/UYQ-21
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	COMPUTER DISPLAY SET
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.940000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.380000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.560000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.100000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.140000E+02

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.260000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.900000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.490000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

DESCRIPTION	SET # 1



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.300000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.200000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.200000E+01
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.300000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.163840E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

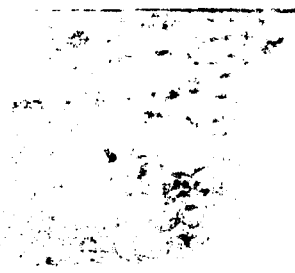
PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.335000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.100000E+08
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.100000E+08	0.0
(2).	WORD LENGTH	0.800000E+01	0.240000E+02
(3).	WORD SEQUENCE LENGTH	0.204800E+04	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.100000E+08	0.100000E+08
(2).	WORD LENGTH	0.100000E+02	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.128000E+03	0.128000E+03
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P80 GROUP



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	PULSED INTERFERENCE DETECTOR
(2).	PCB PART NUMBER (12 CHARACTERS)	1635918
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT COMPANY
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/TPQ-37
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLARY LOCATION RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635705
(8).	PCB ASSEMELY NAME (24 CHARACTERS)	SIGNAL PROCESSOR UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO
INDICATE BY ENTRIES THROUGHOUT. ALSO
INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.800000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.490000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.220000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.800000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.400000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.200000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.0
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.500000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.200000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE ARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.100000E+02

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0 160000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.409600E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.200000E+01

STIMULUS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.175000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01	0.0
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.0	0.0
(3).	CLOCK RATE MAXIMUM	0.100000E+07	0.400000E+07
(4).	PULSE WIDTH	0.0	0.0
(5).	RISE TIME	0.0	0.0
(6).	FALL TIME	0.0	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.0
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.200000E+01	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0	0.0
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.100000E+07	0.400000E+07
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4
(1).	WORD RATE	0.100000E+07	0.0	0.400000E+07	0.0
(2).	WORD LENGTH	0.160000E+02	0.100000E+02	0.140000E+02	0.600000E+01
(3).	WORD SEQUENCE LENGTH	0.0	0.0	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01	0.200000E+01	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.300000E+01	0.300000E+01	0.300000E+01	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0	0.0	0.0	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.400000E+07	0.0
(2).	WORD LENGTH	0.800000E+01	0.140000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0

IF YES, PLEASE ANSWER P80 GROUP

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

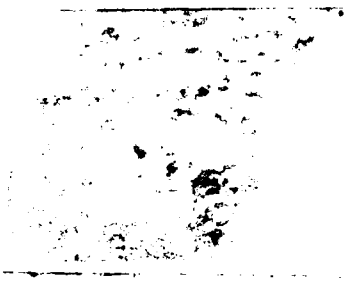
DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	DIGITAL AUTOPILOT
(2).	PCB PART NUMBER (12 CHARACTERS)	390039
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	18876
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	MIRADCOM
(5).	PCB SYSTEM NAME (16 CHARACTERS)	
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.118000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.112000E+03
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.600000E+01
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.100000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.300000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.190000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.220000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.700000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.360000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

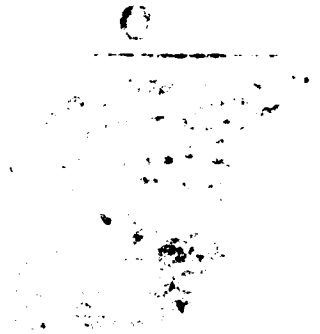
P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.100000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

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P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.130000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL?	
(1).	(NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.400000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.400000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	REED SOLOMON ENCODER
(2).	PCB PART NUMBER (12 CHARACTERS)	1650038
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	JTIDS
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	05869
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	REED SOLOMON ENCODER

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.940000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.600000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.240000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	PCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.120000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.260000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.100000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.480000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.200000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.600000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.512000E+03
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.300000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.300000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.163840E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.102400E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.204800E+04

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCUPACY	0.500000E-01
(3).	MAXIMUM CURRENT DRAIN	0.300000E+01
(4).	RIPPLE PEAK TO PEAK	0.300000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.500000E+07
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.500000E-08
(6).	FALL TIME	0.500000E-08
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTEPNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.500000E+07

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.500000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

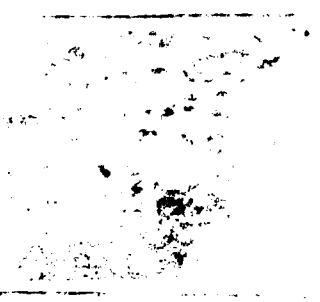
* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.500000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.200000E+01

IF YES, PLEASE ANSWER P80 GROUP



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	REED SOLOMON DECODER
(2).	PCB PART NUMBER (12 CHARACTERS)	1650039
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	JTIDS
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	05869
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	REED SOLOMON DECODER

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.990000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.670000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.220000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.150000E+02

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.120000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.190000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.460000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.300000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.200000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.600000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.160000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.212480E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.104800E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.614400E+04

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

DESCRIPTION	SET # 1
(15). CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(16). HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17). WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

DESCRIPTION	SET # 1
(1). DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2). DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3). DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4). DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5). DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCUPACY	0.500000E-01
(3).	MAXIMUM CURRENT DRAIN	0.350000E+01
(4).	RIPPLE PEAK TO PEAK	0.300000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.500000E+07
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.500000E-08
(6).	FALL TIME	0.500000E-08
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.500000E+07

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.500000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.500000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P80 GROUP

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	DIGITAL AUTOPILOT NO.1
(2).	PCB PART NUMBER (12 CHARACTERS)	390037
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	18876
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	MIRADCOM
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AUTOPILOT
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.620000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.310000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.470000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.200000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.160000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.140000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.300000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS & LOOPS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: 1 = NONE
2 = MINOR (LESS THAN 10% OF IC'S INVOLVED)
3 = MEDIUM (10%-25% OF IC'S INVOLVED)
4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)

	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.200000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.200000E+01
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

DESCRIPTION	SET # 1

(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.100000E+02

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.200000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.409600E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.160000E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.102400E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.409600E+04

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

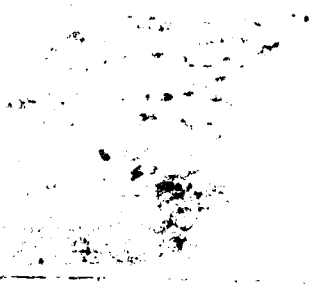
PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.500000E+01
(3).	MAXIMUM CURRENT DRAIN	0.190000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.100000E+01
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTEPNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.160000E+02	0.100000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.200000E+01	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.160000E+02	0.100000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0

IF YES, PLEASE ANSWER P80 GROUP



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	PROGRAM MEMORY
(2).	PCB PART NUMBER (12 CHARACTERS)	D3567251
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	82577
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	PHOENIX
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	PHOENIX MISSLE SYSTEM
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.116000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.470000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.470000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.900000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.210000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.480000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.100000E+01
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.780000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GPOUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS? ...	0.200000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.200000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.480000E+02

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01	0.0	0.0
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01	0.0	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.200000E+01	0.300000E+01	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.100000E+01	0.0	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01	0.0	0.0
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01	0.0	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01	0.0	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01	0.0	0.0
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.819200E+04	0.0	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.395000E+06	0.0	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01	0.0	0.0
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0	0.0	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0	0.0	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0	0.0	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

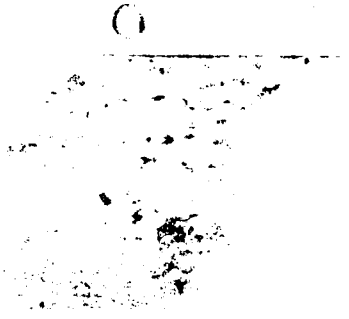
PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0	0.0	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0	0.0	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0	0.0	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * *DIGITAL PCB TEST REQUIREMENTS SUMMARY* * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.500000E+01
(3).	MAXIMUM CURRENT DRAIN	0.100000E+02
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.140000E+02	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.200000E+01	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.0
(2).	WORD LENGTH	0.240000E+02
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P78 GROUP

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.0
(3).	WORD SEQUENCE LENGTH	0.240000E+02
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1
IF YES, PLEASE ANSWER P80 GROUP	



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	131072 BIT MEMORY
(2).	PCB PART NUMBER (12 CHARACTERS)	3177422
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/UYQ-21
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	RADAR DISPLAY UNIT
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	3177420
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	131072 BIT MEMORY

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO
INDICATE BY ENTRIES THROUGHOUT. ALSO
INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.820000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.440000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.200000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.110000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.0
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.320000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.430000E+02

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01
(4)	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.100000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * OIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	WHAT IS THE MAXIMUN SIZE OF THE LARGEST RAM?	0.409600E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.131000E+06
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.200000E-02

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01	0.150000E+02	-.150000E+02
(2).	ACCURACY	0.500000E+01	0.500000E+01	0.500000E+01
(3).	MAXIMUM CURRENT DRAIN	0.100000E+01	0.150000E+01	0.100000E+00
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.500000E+07
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.100000E-06
(5).	RISE TIME	0.200000E-07
(6).	FALL TIME	0.200000E-07
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
	# OF CLOCK PULSE PHASES APPLIED	0.0
	[illegible] (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.500000E+07
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAl CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.200000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.500000E+07
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P80 GROUP



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	32K-16 RAM
(2).	PCB PART NUMBER (12 CHARACTERS)	1646310
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/UYQ-21
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	RADAR DISPLAY UNIT
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1646310
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	32K-16RAM

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.960000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.580000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.160000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.300000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.120000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.320000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.470000E+02

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.100000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.160000E+05
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.262000E+06
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.200000E-02

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01	0.150000E+02	-.150000E+02
(2).	ACCURACY	0.500000E+01	0.500000E+01	0.500000E+01
(3).	MAXIMUM CURRENT DRAIN	0.280000E+00	0.400000E+00	0.150000E-01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.100000E+08
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.350000E-07
(6).	FALL TIME	0.350000E-07
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.100000E+08
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.100000E+08
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.200000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.100000E+08
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.200000E+01
(6).	IS THERE A SYNCHPONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P80 GROUP



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

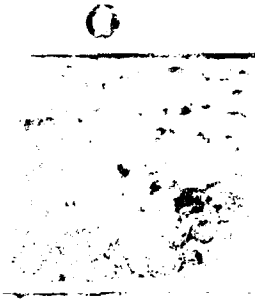
DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

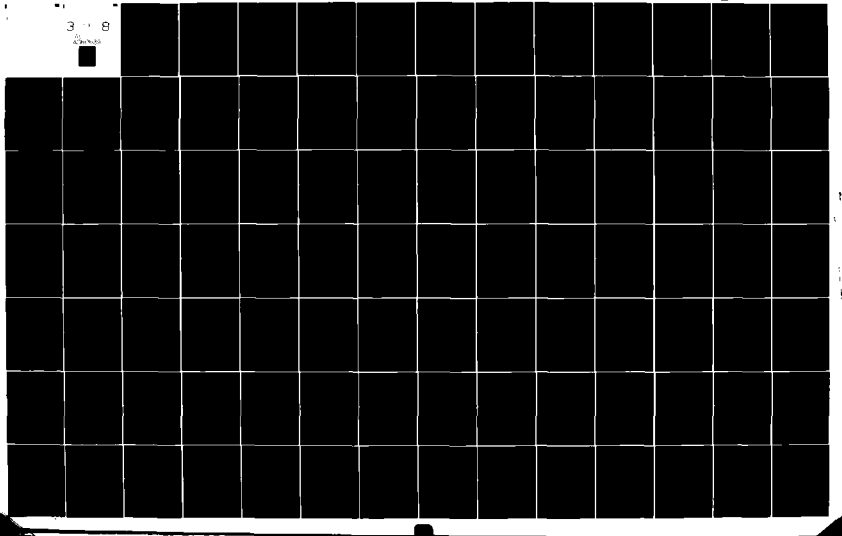
	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	ARITHMETIC UNIT
(2).	PCB PART NUMBER (12 CHARACTERS)	3523201
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	82577
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AWG-9 /AIM-54
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	PHOENIX MISSILE SYSTEM
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



AD-A080 839 HUGHES AIRCRAFT CO FULLERTON CA GROUND SYSTEMS GROUP F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
AUG 79 DAAK40-78-C-0290
UNCLASSIFIED HAC-FR79-12-669A NL



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIPEMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1	SET # 2
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.283000E+03	0.283000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.157000E+03	0.157000E+03
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.970000E+02	0.970000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)		
(5).	TTL	0.200000E+01	0.200000E+01
(6).	CTL	0.100000E+01	0.100000E+01
(7).	RTL	0.100000E+01	0.100000E+01
(8).	DTL	0.100000E+01	0.100000E+01
(9).	IIL	0.100000E+01	0.100000E+01
(10).	ECL	0.100000E+01	0.100000E+01
(11).	DCTL	0.100000E+01	0.100000E+01
(12).	RCTL	0.100000E+01	0.100000E+01
(13).	HNIL	0.100000E+01	0.100000E+01
(14).	CMOS	0.100000E+01	0.100000E+01
(15).	NMOS	0.100000E+01	0.100000E+01
(16).	PMOS	0.100000E+01	0.100000E+01
(17).	EIA	0.100000E+01	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01	0.100000E+01
(19).	OTHER	0.100000E+01	0.100000E+01
(20).	NUMBER OF SSI	0.170000E+02	0.170000E+02

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(21).	NUMBER OF MSI	0.186000E+03	0.186000E+03
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.400000E+01	0.400000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.207000E+03	0.207000E+03

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1	SET # 2

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)		
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)		
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,		
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0	0.0
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)		
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.300000E+01	0.300000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,		
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01	0.100000E+01

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1	SET # 2
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01	0.100000E+01
	(NO=1,YES=2)		
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.500000E+01	0.500000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1	SET # 2
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01	0.200000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.256000E+03	0.256000E+03
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.102400E+04	0.102400E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

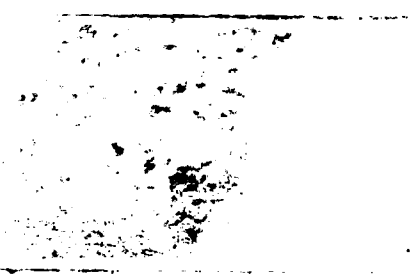
PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0	0.0
(16).	HOW? (PRESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1	SET # 2
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01	0.100000E+01

STIMULUS



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01	0.500000E+01
(2).	ACCURACY	0.300000E+01	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.250000E+02	0.250000E+02
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.0	0.0
(3).	CLOCK RATE MAXIMUM	0.0	0.0
(4).	PULSE WIDTH	0.0	0.0
(5).	RISE TIME	0.0	0.0
(6).	FALL TIME	0.0	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.240000E+02	0.240000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.240000E+02	0.240000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0	0.0

IF YES, PLEASE ANSWER P80 GROUP



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	FILTER DOPPLER
(2).	PCB PART NUMBER (12 CHARACTERS)	1635910
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/TPQ-37
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLERY LOCATION RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635705
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	SIGNAL PROCESSING UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO
INDICATE BY ENTRIES THROUGHOUT. ALSO
INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



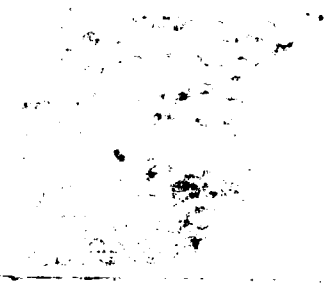
PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.100000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.460000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.390000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.500000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.230000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.900000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.370000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.400000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.500000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.150000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.200000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.100000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

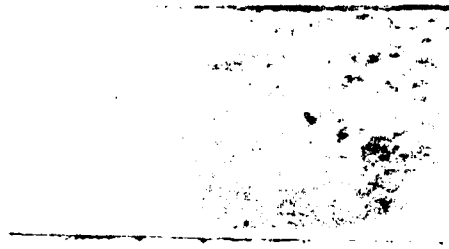
(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.265000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.250000E-07
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.100000E+01
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.310000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.200000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P80 GROUP

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	GENERATOR,SYNC,CLOCK/TV.
(2).	PCB PART NUMBER (12 CHARACTERS)	1635884
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/TPQ-37
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLERY LOCATION RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635705
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	SIGNAL PROCESSOR UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.990000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.400000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.510000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.100000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.250000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.500000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.400000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

DESCRIPTION	SET # 1
NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) (1). DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.400000E+01
(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, (2). CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) (3). DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, (4). CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

DESCRIPTION	SET # 1
(1). DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(NO=1,YES=2) (2). DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3). DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

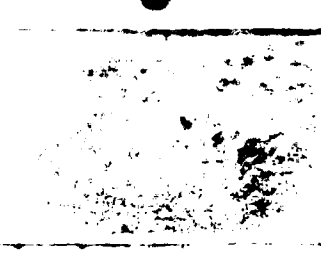
	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.400000E+01

PARAMETER GROUP: P62 (DIGITAL CHARACTERISTICS - ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE ONE-SHOT DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN ONE-SHOT(S) BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(3).	EDGE TRIGGERED? (POSITIVE=1,NEGATIVE=2)	0.100000E+01
	WHAT IS THE DELAY (PULSE WIDTH) OF THE ONE-SHOTS?	
(4).	DELAY MINIMUM	0.440000E-04
(5).	DELAY MAXIMUM	0.419000E+00

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01	0.200000E+01	0.200000E+01



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01	0.200000E+01	0.200000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.200000E+01	0.200000E+01	0.200000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.100000E+01	0.100000E+01	0.100000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.760000E+03	0.524000E+03	0.150000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01	0.200000E+01	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.102400E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCUPACY	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.270000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2
	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL?		
(1).	(NO=1,YES=2)	0.100000E+01	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.		
(2).	CLOCK RATE MINIMUM	0.0	0.0
(3).	CLOCK RATE MAXIMUM	0.0	0.0
(4).	PULSE WIDTH	0.0	0.0
(5).	RISE TIME	0.0	0.0
(6).	FALL TIME	0.0	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.200000E+01	0.100000E+01
	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS		
(11).	OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01	0.0
	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE		
(12).	EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01	0.0
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2

NOTE: THEPE IS NO P69 GPOUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.180000E+02
(3).	*WORD SEQUENCE LENGTH*	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.180000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P80 GROUP

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	CONTROL COMPUTER MESSAGE
(2).	PCB PART NUMBER (12 CHARACTERS)	1635883
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/TPQ-37
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLERY LOCATION RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635705
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	SIGNAL PROCESSOR UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

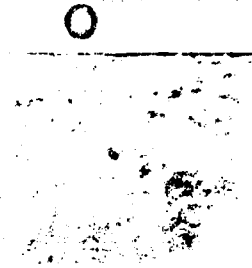
PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.100000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.530000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.370000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.220000E+02



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

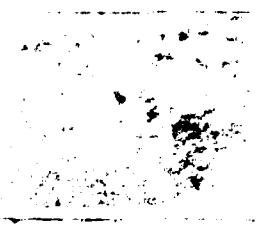
(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.450000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.100000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.460000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

DESCRIPTION	SET # 1



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.400000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.0

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.128000E+03
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1	SET # 2
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01	0.0
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.200000E+01	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01	0.0
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01	0.0
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.204800E+04	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01	0.0
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.200000E+01

STIMULUS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.950000E+00
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - *PARALLEL INPUT CHARACTERISTICS*)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.180000E+02
(3).	*WORD SEQUENCE LENGTH*	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVEL(S)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.500000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P80 GROUP

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

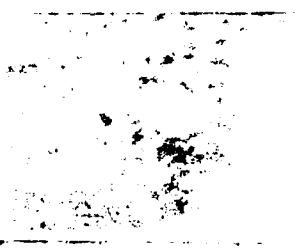
DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCPIPTION (32 CHARACTERS)	DISCRETE FOURIER TRANSFORM
(2).	PCB PART NUMBER (12 CHARACTERS)	3567221
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	82577
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT COMPANY
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AGW-9/AIM-54
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	PHOENIX MISSILE SYSTEM
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1	SET # 2
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.140000E+03	0.100000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.190000E+02	0.400000E+01
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.820000E+02	0.820000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01	0.0
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)		
(5).	TTL	0.200000E+01	0.0
(6).	CTL	0.100000E+01	0.0
(7).	RTL	0.100000E+01	0.0
(8).	DTL	0.100000E+01	0.0
(9).	IIL	0.100000E+01	0.0
(10).	ECL	0.100000E+01	0.0
(11).	DCTL	0.100000E+01	0.0
(12).	RCTL	0.100000E+01	0.0
(13).	HNIL	0.100000E+01	0.0
(14).	CMOS	0.100000E+01	0.0
(15).	NMOS	0.100000E+01	0.0
(16).	PMOS	0.100000E+01	0.0
(17).	EIA	0.100000E+01	0.0
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01	0.0
(19).	OTHER	0.100000E+01	0.0
(20).	NUMBER OF SSI	0.260000E+02	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(21).	NUMBER OF MSI	0.340000E+02	0.0
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.220000E+02	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.500000E+01	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01	0.0
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.300000E+01	0.0
(26).	PCB COMPLEXITY FACTOR	0.0	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01	0.0
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01	0.0
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01	0.0
(30).	TOTAL NUMBER OF IC'S ON PCB	0.870000E+02	0.0

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1

NOTE: 1 = NONE
2 = MINOR (LESS THAN 10% OF IC'S INVOLVED)
3 = MEDIUM (10%-25% OF IC'S INVOLVED)
4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)

	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.400000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.400000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.0
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.819200E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.512000E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.102400E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.112600E+05

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)	0.200000E+01
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)	0.200000E+01
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)	0.0
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)	0.290100E+04
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)	
(5).	PIA	0.0
(6).	ACIA	0.0
(7).	PLA	0.0
(8).	UART	0.0
(9).	SAT	0.0
(10).	SAR	0.0
(11).	OTHER	0.0
(12).	OTHER	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	INFORMATION ON SUPPORT CHIPS:	
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)	0.0
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS	
	CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE	
(14).	MICROPROCESSOR? (NO=1,YES=2)	0.0
	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF	
(15).	EACH OTHER? (NO=1,YES=2)	0.0
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)	0.0
	INFORMATION ON THE MICROPROCESSORS:	
(17).	QUANTITY	0.400000E+01
	DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST	
(18).	POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
	IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM	
(19).	TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
	CAN CONTROL LINES ON MICROPROCESSOR BE DISABLED FROM TEST POINTS	
(20).	OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
	MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2)	
(21).	ROM	0.100000E+01
(22).	STATIC RAM	0.200000E+01
(23).	DYNAMIC RAM	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(24).	CAN MICROPROCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2)	0.100000E+01

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.300000E+01
(3).	MAXIMUM CURRENT DRAIN	0.100000E+02
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.300000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.600000E+01	0.700000E+01
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	WORD RATE	0.0	0.0	0.0
(2).	WORD LENGTH	0.160000E+02	0.800000E+01	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.0	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01	0.100000E+01	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01	0.100000E+01

IF YES, PLEASE ANSWER P80 GROUP

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	16 BIT MICROPROCESSOR
(2).	PCB PART NUMBER (12 CHARACTERS)	1633050
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	HMD-22
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.404000E-03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.100000E+03
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.140000E+03
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.570000E+02

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.730000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.500000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.400000E+01
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.139000E+03

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STPUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.100000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.160000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.716800E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)	0.200000E+01
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)	0.200000E+01
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)	0.0
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)	0.290100E+04
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)	
(5).	PIA	0.0
(6).	ACIA	0.0
(7).	PLA	0.0
(8).	UART	0.0
(9).	SAT	0.0
(10).	SAR	0.0
(11).	OTHER	0.0
(12).	OTHER	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	INFORMATION ON SUPPORT CHIPS:	
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS	
	CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE	
(14).	MICROPROCESSOR? (NO=1,YES=2)	0.0
	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF	
(15).	EACH OTHER? (NO=1,YES=2)	0.0
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)	0.100000E+01
	INFORMATION ON THE MICROPROCESSORS:	
(17).	QUANTITY	0.400000E+01
	DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST	
(18).	POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
	IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM	
(19).	TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
	CAN CONTROL LINES ON MICROPROCESSOR BE DISABLED FROM TEST POINTS	
(20).	OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
	MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2)	
(21).	ROM	0.200000E+01
(22).	STATIC RAM	0.200000E+01
(23).	DYNAMIC RAM	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

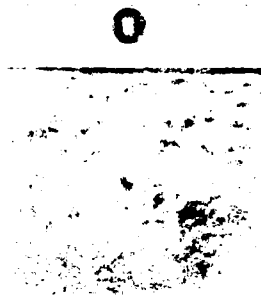
PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(24).	CAN MICPOFROCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.100000E+00
(3).	MAXIMUM CURRENT DRAIN	0.101000E+02
(4).	RIPPLE PEAK TO PEAK	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.100000E+01
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.300000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.150000E+08

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.300000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P71 (DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.0
(2).	WORD LENGTH	0.200000E+01
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P72 GROUP

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	WORD RATE	0.0	0.0	0.0
(2).	WORD LENGTH	0.110000E+02	0.160000E+02	0.320000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1	SET # 2	SET # 3
IF YES, PLEASE ANSWER P74 GROUP			

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.300000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.200000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.0
(2).	WORD LENGTH	0.200000E+01
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS) - CONTINUED -

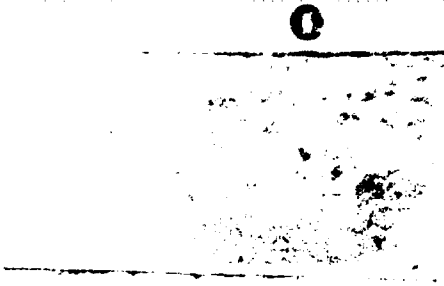
	DESCRIPTION	SET # 1
(6).	IS THERE A SYNCHRONIZATION' REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P78 GROUP

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2
(1).	WORD RATE	0.0	0.0
(2).	WORD LENGTH	0.320000E+02	0.320000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0	0.0

IF YES, PLEASE ANSWER P80 GROUP



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	DECISION LOGIC MULTINET
(2).	PCB PART NUMBER (12 CHARACTERS)	1650036
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05869
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	JTIDS
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	05869
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	DECISION LOGIC MULTINET

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.990000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.660000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.250000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.150000E+02

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(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.230000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.500000E+01
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.430000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.200000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.100000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.100000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.0
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.160000E+02
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.300000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.100000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.300000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.204800E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.600000E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.102400E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.640000E+02
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES) - CONTINUED -

DESCRIPTION	SET # 1
STIMULUS	
PARAMETER GROUP: P67 (POWER SUPPLY)	
DESCRIPTION	SET # 1
(1). POLARITIES/VOLTAGE(S)	0.500000E+01
(2). ACCURACY	0.500000E+01
(3). MAXIMUM CURRENT DRAIN	0.300000E+01
(4). RIPPLE PEAK TO PEAK	0.300000E+00
PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)	
DESCRIPTION	SET # 1
ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2) (1).	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.500000E+07
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.500000E-08
(6).	FALL TIME	0.500000E-08
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.500000E+07



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PARAMETER GROUP: P71 (DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.500000E+07
(2).	WORD LENGTH	0.120000E+02
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P71 (DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.200000E+01

IF YES, PLEASE ANSWER P72 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * *DIGITAL PCB TEST REQUIREMENTS SUMMARY* * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	DIGITAL AUTOPILOT 2
(2).	PCB PART NUMBER (12 CHARACTERS)	390038
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	18876
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	MIRADCOM
(5).	PCB SYSTEM NAME (16 CHARACTERS)	
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	18876
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	DIGITAL AUTOPILOT 2

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO
INDICATE BY ENTRIES THROUGHOUT. ALSO
INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.105000E+03
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.250000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.760000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.700000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.200000E+01
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.130000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.200000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.260000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.400000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.200000E+01
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.120000E+02

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.400000E+01
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.409600E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.530000E+05
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.100000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.0
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.0
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)	0.200000E+01
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)	0.200000E+01
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)	0.0
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)	0.670100E+04
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)	
(5).	PIA	0.0
(6).	ACIA	0.0
(7).	PLA	0.0
(8).	UART	0.0
(9).	SAT	0.0
(10).	SAR	0.0
(11).	OTHER	0.0
(12).	OTHER	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	INFORMATION ON SUPPORT CHIPS:	
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)	0.0
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS	
	CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE	
(14).	MICROPROCESSOR? (NO=1,YES=2)	0.0
	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF	
(15).	EACH OTHER? (NO=1,YES=2)	0.0
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)	0.0
	INFORMATION ON THE MICROPROCESSORS:	
(17).	QUANTITY	0.400000E+01
	DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST	
(18).	POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.200000E+01
	IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM	
(19).	TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
	CAN CONTROL LINES ON MICROPPOCESSOR BE DISABLED FROM TEST POINTS	
(20).	OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
	MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2)	
(21).	ROM	0.200000E+01
(22).	STATIC RAM	0.200000E+01
(23).	DYNAMIC RAM	0.100000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(24).	CAN MICROPROCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01
(2).	ACCURACY	0.500000E+01
(3).	MAXIMUM CURRENT DRAIN	0.350000E+01
(4).	RIPPLE PEAK TO PEAK	0.300000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.600000E+07
(4).	PULSE WIDTH	0.500000E-07
(5).	RISE TIME	0.500000E-08
(6).	FALL TIME	0.500000E-08
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIPEMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.600000E+07

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.550000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.600000E+07
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.200000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1
IF YES, PLEASE ANSWER P80 GROUP	



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	MEMORY
(2).	PCB PART NUMBER (12 CHARACTERS)	1642182
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05669
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	TPQ-36
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLERY LOCATING RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635705
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	SIGNAL PROCESSING UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO
INDICATE BY ENTRIES THPOUGHOUT. ALSO
INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.710000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.370000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.180000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.400000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.430000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.200000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.0
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.470000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

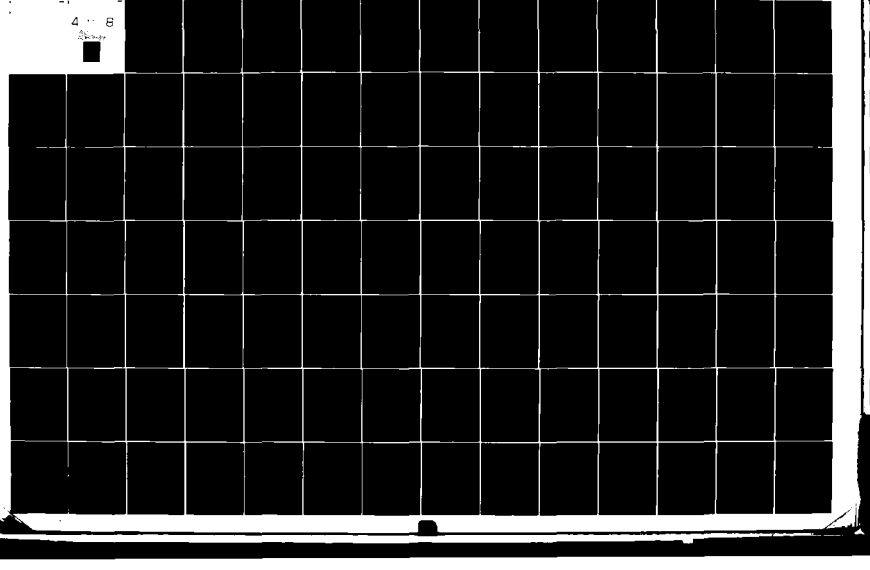
PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

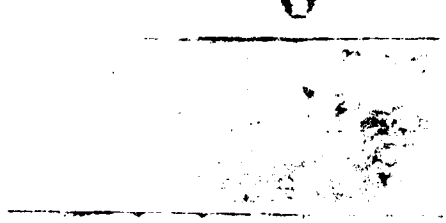
(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.100000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.0
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.0
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.409600E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.737280E+05



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.100000E-02

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.100000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS

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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01	-.500000E+01	0.120000E+02
(2).	ACCURACY	0.100000E+02	0.100000E+02	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.570000E+00	0.350000E-02	0.240000E+01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.100000E+04
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.500000E-03
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.100000E+04
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.220000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.600000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	WORD RATE	0.100000E+04	0.100000E+04	0.100000E+04
(2).	WORD LENGTH	0.100000E+02	0.120000E+02	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0	0.0	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0	0.0	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.100000E+04
(2).	WORD LENGTH	0.160000E+02
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P80 GROUP



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

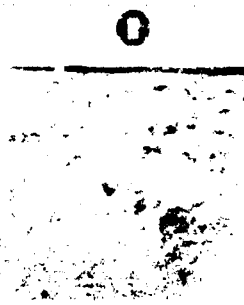
DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	MICROPROCESSOR
(2).	PCB PART NUMBER (12 CHARACTERS)	1635972
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	05096
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	HUGHES AIRCRAFT CO.
(5).	PCB SYSTEM NAME (16 CHARACTERS)	AN/TPQ-37
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	ARTILLARY LOCATING RADAR
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	1635205
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	SIGNAL PROCESSING UNIT

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



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* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.970000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.170000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.690000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.130000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.110000E+02
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.300000E+01
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.290000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
	NOTE: 1 = NONE 2 = MINOR (LESS THAN 10% OF IC'S INVOLVED) 3 = MEDIUM (10%-25% OF IC'S INVOLVED) 4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)	
(1).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(2).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0
(3).	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4) DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
(4).	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1, CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	(NO=1,YES=2) DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.200000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STPUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.200000E+01

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE FLIP-FLOP DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, CAN THE FLIP-FLOPS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(3).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(4).	ARE FLIP-FLOPS SYNCHRONOUSLY CLOCK TRIGGERED? (NO=1,YES=2)	0.0
(5).	DOES PCB HAVE REGISTERS? (NO=1,YES=2)	0.100000E+01
(6).	IF YES, CAN THE REGISTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.0
(7).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.0
(8).	DOES PCB HAVE ROMS? (NO=1,YES=2)	0.200000E+01
(9).	WHAT IS THE MAXIMUM SIZE OF ROM?	0.102400E+04
(10).	INDICATE TOTAL QUANTITY OF ROM BITS USED	0.204800E+04
(11).	DOES PCB HAVE RAMS? (NO=1,YES=2)	0.200000E+01
(12).	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?	0.102400E+04
(14).	INDICATE TOTAL QUANTITY OF RAM BITS USED	0.898200E+04

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P64 (DIGITAL CHARACTERISTICS - STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(15).	CAN RAM'S BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(16).	HOW? (RESET=1,PRESET=2,CLOCK=3,CLEAR=4,OTHER=5)	0.500000E+01
(17).	WHAT IS THE REFRESH RATE OF DYNAMIC RAM'S?	0.0

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)	0.200000E+01
(2).	IS MICROPROCESSOR SOCKET MOUNTED OR HARD WIRED? (SM=1,HW=2)	0.100000E+01
(3).	WHAT IS MANUFACTURER'S NAME? (24 CHARACTERS)	0.0
(4).	WHAT IS MANUFACTURER'S MODEL NUMBER? (12 CHARACTERS)	0.808000E+04
	HOW MANY OF THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS ARE ON THE BOARD? (INDICATE NUMBER)	
(5).	PIA	0.0
(6).	ACIA	0.0
(7).	PLA	0.0
(8).	UART	0.0
(9).	SAT	0.0
(10).	SAR	0.0
(11).	OTHER	0.0
(12).	OTHER	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	INFORMATION ON SUPPORT CHIPS:	
(13).	ARE THE SUPPORT CHIPS TRISTATABLE? (NO=1,YES=2)	0.200000E+01
	IF YES, PLEASE ANSWER NEXT TWO QUESTIONS CAN EACH SUPPORT CHIP BE TRISTATED INDEPENDENTLY OF THE	
(14).	MICROPROCESSOR? (NO=1,YES=2)	0.200000E+01
	CAN ALL SUPPORT CHIPS BE TRISTATED INDEPENDENTLY OF	
(15).	EACH OTHER? (NO=1,YES=2)	0.200000E+01
(16).	ARE ANY SUPPORT CHIPS SOCKET MOUNTED? (NO=1,YES=2)	0.100000E+01
	INFORMATION ON THE MICROPROCESSORS:	
(17).	QUANTITY	0.100000E+01
	DOES PCB HAVE ACCESS TO MICROPROCESSOR CONTROL LINES FROM TEST	
(18).	POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3) ..	0.300000E+01
	IF YES, CAN CONTROL LINES ON MICROPROCESSOR BE INITIALIZED FROM	
(19).	TEST POINTS OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
	CAN CONTROL LINES ON MICROPROCESSOR BE DISABLED FROM TEST POINTS	
(20).	OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
	MEMORY ELEMENT(S) USED WITHIN MICROPROCESSOR? (NO=1,YES=2)	
(21).	ROM	0.100000E+01
(22).	STATIC RAM	0.0
(23).	DYNAMIC RAM	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P65 (DIGITAL CHARACTERISTICS - MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(24).	CAN MICROPROCESSOR OUTPUT (BUS) LINES BE FORCED INTO TRISTATE? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.200000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.100000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.100000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.100000E+01

STIMULUS



P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S)	0.120000E+02	0.500000E+01	-.500000E+01
(2).	ACCURACY	0.100000E+02	0.100000E+02	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.920000E-01	0.270000E+01	0.100000E-02
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00	0.200000E+00

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS. CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.0
(4).	PULSE WIDTH	0.0
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.0
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.0
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(11).	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.100000E+01
(12).	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.100000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.130000E+02	0.500000E+01	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01	0.850000E+01	0.280000E+01	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00	0.800000E+00	0.800000E+00	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0	-.100000E+01	0.0	-.500000E+00
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0	0.0	0.0	0.0
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0	0.0	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.200000E+07
(2).	WORD LENGTH	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.240000E+04
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01	0.370000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.450000E+00	0.450000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0	0.0
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.100000E+01
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.200000E+07
(2).	WORD LENGTH	0.800000E+01
(3).	WORD SEQUENCE LENGTH	0.240000E+04
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.0
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P80 GROUP

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

DIGITAL PCB CARD IDENTIFICATION

PARAMETER GROUP: P57 (PCB IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	PCB DESCRIPTION (32 CHARACTERS)	DIGITAL AUTOPILOT
(2).	PCB PART NUMBER (12 CHARACTERS)	390040
(3).	PCB MANUFACTURER'S CODE (12 CHARACTERS) ..	18876
(4).	PCB MANUFACTURER'S NAME (24 CHARACTERS) ..	MIRADCOM
(5).	PCB SYSTEM NAME (16 CHARACTERS)	
(6).	PCB SYSTEM DESCRIPTION (32 CHARACTERS)	
(7).	PCB ASSEMBLY CODE (12 CHARACTERS)	
(8).	PCB ASSEMBLY NAME (24 CHARACTERS)	

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

DIGITAL CHARACTERISTICS



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?	0.590000E+02
(2).	NUMBER OF PCB PINS WHICH REQUIRE DIGITAL INPUTS	0.460000E+02
(3).	NUMBER OF PCB PINS WHICH OUTPUT DIGITAL SIGNALS	0.130000E+02
(4).	LOGIC TRI-STATE PRESENT? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES USED ON PCB (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.100000E+01
(8).	DTL	0.100000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.100000E+01
(15).	NMOS	0.100000E+01
(16).	PMOS	0.100000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	NUMBER OF SSI	0.900000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P58 (DIGITAL CHARACTERISTICS - GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(21).	NUMBER OF MSI	0.110000E+02
(22).	NUMBER OF LSI WITH 24 PINS/PACKAGE	0.0
(23).	NUMBER OF LSI WITH MORE THAN 24 PINS/PACKAGE	0.0
(24).	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)	0.100000E+01
(25).	IS PCB DESIGNED FOR TESTABILITY? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(26).	PCB COMPLEXITY FACTOR	0.0
(27).	DIGITAL FORMAT (RZ=1,NRZ=2,OTHER=5)	0.100000E+01
(28).	CAN PCB DEVICES BE INITIALIZED AT TEST POINT AND/OR EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.200000E+01
(29).	ARE COMPONENTS AC COUPLED? (NONE=1,SOME=2,ALL=3)	0.100000E+01
(30).	TOTAL NUMBER OF IC'S ON PCB	0.200000E+02

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS)

	DESCRIPTION	SET # 1

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P60 (DIGITAL CHARACTERISTICS - LOOPS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: 1 = NONE
2 = MINOR (LESS THAN 10% OF IC'S INVOLVED)
3 = MEDIUM (10%-25% OF IC'S INVOLVED)
4 = MAJOR (MORE THAN 25% OF IC'S INVOLVED)

	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(1).	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(2).	CAN SYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0
	SPECIFY (NONE=1,MINOR=2,MEDIUM=3,MAJOR=4)	
(3).	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?	0.100000E+01
	(NONE=1,SOME=2,ALL=3) IF PREVIOUS QUESTION IS NOT 1,	
(4).	CAN ASYNCHRONOUS LOOPS BE BROKEN OR INTERRUPTED?	0.0

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES))

DESCRIPTION	SET # 1

(1).	DOES PCB HAVE LARGE (>10) FAN-IN CONNECTIONS? (NO=1,YES=2)	0.100000E+01
	(NO=1,YES=2)	
(2).	DOES ANY IC ON THE BUS BOTH REC/X-MIT DATA FROM/TO THE BUS?	0.100000E+01
(3).	DOES PCB HAVE BUSES ON THE EDGE CONNECTOR? (NO=1,YES=2) ..	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P61 (DIGITAL CHARACTERISTICS - WIRED AND (BUSES)) - CONTINUED -

	DESCRIPTION	SET # 1
(4).	DOES PCB HAVE INTERNAL BUS STRUCTURE? (LIST MAXIMUM NUMBER OF IC'S INVOLVED ON ONE BUS NODE)	0.100000E+01

PARAMETER GROUP: P63 (DIGITAL CHARACTERISTICS - COUNTERS)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE COUNTERS? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAN COUNTERS BE INITIALIZED FROM EITHER TEST POINTS OR THE EDGEBOARD CONNECTOR? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(3).	ARE TWO OR MORE COUNTER IC'S CONNECTED IN SERIES? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, ARE THERE ACCESS POINTS BETWEEN COUNTER IC'S? (NONE=1,SOME=2,ALL=3)	0.300000E+01
(5).	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)	0.256000E+03
(6).	WHAT IS THE RADIX (BASE) OF THE COUNTERS?	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P66 (DIGITAL CHARACTERISTICS - COMBINATIONAL DEVICES)

	DESCRIPTION	SET # 1
(1).	DOES PCB HAVE DECODER/DEMULTIPLEXER DEVICES? (NO=1,YES=2)	0.100000E+01
(2).	DOES PCB HAVE ENCODER/MULTIPLEXER DEVICES? (NO=1,YES=2) ..	0.200000E+01
(3).	DOES PCB HAVE BINARY ADDERS? (NO=1,YES=2)	0.200000E+01
(4).	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)	0.200000E+01
(5).	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)	0.200000E+01

STIMULUS

PARAMETER GROUP: P67 (POWER SUPPLY)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S)	0.500000E+01	0.150000E+02	-.150000E+02
(2).	ACCURACY	0.100000E+02	0.100000E+02	0.100000E+02
(3).	MAXIMUM CURRENT DRAIN	0.700000E+00	0.340000E-01	0.340000E-01
(4).	RIPPLE PEAK TO PEAK	0.200000E+00	0.200000E+00	0.200000E+00

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES)

	DESCRIPTION	SET # 1
	ARE ANY OF THE FOLLOWING CLOCK PARAMETERS CRITICAL?	
(1).	(NO=1,YES=2)	0.100000E+01
	IF YES, PLEASE ANSWER NEXT 5 QUESTIONS.	
(2).	CLOCK RATE MINIMUM	0.0
(3).	CLOCK RATE MAXIMUM	0.800000E+07
(4).	PULSE WIDTH	0.125000E-06
(5).	RISE TIME	0.0
(6).	FALL TIME	0.0
(7).	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE REQUIRED?	0.100000E+01
(9).	NUMBER OF CLOCK PULSE PHASES APPLIED	0.100000E+01
(10).	DOES PCB HAVE INTERNAL CLOCK(S)? (NO=1,YES=2)	0.100000E+01
	CAN INTERNAL CLOCK BE INHIBITED FROM EITHER TEST POINTS	
(11).	OR THE EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.0
	CAN EXTERNAL CLOCK BE APPLIED AT EITHER TEST POINTS OR THE	
(12).	EDGEBOARD CONNECTOR? (NO=1,YES=2)	0.200000E+01
(13).	WHAT IS THE EXTERNAL CLOCK RATE MINIMUM?	0.0
(14).	WHAT IS THE EXTERNAL CLOCK RATE MAXIMUM?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P68 (DIGITAL CHARACTERISTICS - CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1

NOTE: THERE IS NO P69 GROUP. THE TESTER PARAMETERS IN T69 WILL BE MATCHED TO P72 AND P74.

PARAMETER GROUP: P70 (DIGITAL CHARACTERISTICS - LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.400000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P73 (DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.0

IF YES, PLEASE ANSWER P74 GROUP

PARAMETER GROUP: P76 (DIGITAL CHARACTERISTICS - OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.150000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01	0.900000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.400000E+00	-.900000E+01
(4).	LOGIC LEVEL "0" MINIMUM	0.0	-.150000E+02
(5).	OUTPUT LOAD(S) REQUIRED (NO=1,YES=2)	0.100000E+01	0.0
(6).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01	0.0
(7).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P77 (DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE	0.370000E+02
(2).	WORD LENGTH	0.0
(3).	SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.0
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

IF YES, PLEASE ANSWER P78 GROUP

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE	0.0
(2).	WORD LENGTH	0.400000E+01
(3).	WORD SEQUENCE LENGTH	0.0
(4).	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)	0.100000E+01
(5).	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?	0.100000E+01
(6).	IS THERE A SYNCHRONIZATION REQUIREMENT? (NO=1,YES=2)	0.100000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TEST REQUIREMENTS SUMMARY * * *

(TABULATION BY PCB)

PARAMETER GROUP: P79 (DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1
IF YES, PLEASE ANSWER P80 GROUP	



INTERIM REPORT ATT II – MM&T – DFI FOR PCBs – FI TEST SYSTEM SURVEY

FAULT ISOLATION TEST SYSTEM SURVEY –

ATTACHMENT II TO INTERIM REPORT (BASIC EFFORT)

MANUFACTURING METHODS AND TECHNOLOGY FOR 'DIGITAL FAULT ISOLATION FOR PRINTED CIRCUIT BOARDS'

PROJECT NO. R783242

CONTRACT DAAK40-78-C-0290
25 AUGUST 1979
CDRL A003

FR 79-12-669
99230

FAULT ISOLATION TEST SYSTEM SURVEY

ATTACHMENT II

TO INTERIM REPORT (BASIC EFFORT)

Manufacturing Methods and Technology for

'Digital Fault Isolation for Printed Circuit Boards'

Project No. R783242

Prepared for

U.S. Army Missile Research and Development Command

Redstone Arsenal, Alabama 35809

Project Officer: G. Little
DRDMI-EAT
(205)-876-3848

Contract No. DAAK 40-78-C-0290
CDRL A003

Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

Report Date: 25 August 1979
FR79-12-669

FOREWORD

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards contraining complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the development of digital fault isolation methodology, and the identification of the corresponding optimum available automatic test hardware.

The subsequent contract option phase of this project involves the purchase, setup, and demonstration of the selected fault isolation hardware/software system, using the developed techniques.

CONTENTS

Section IIA – Tester Questionnaire
Section IIB – D/PCB Tester Capability Summary
Section IIC – D/PCB Test System Specification

SECTION IIA
TESTER QUESTIONNAIRE

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MM    MM  IIIIIII  RRRRRR    AAAAA   DDDDDD    CCCCC    OOOOO  M     M
MM   MM     I     R     R  A     A  D     D  C     C  O     O MM   MM
M M M M     I     R     R  A     A  D     D  C        O     O M M M M
M  M  M     I     RRRRRR   AAAAAAA  D     D  C        O     O M  M  M
M     M     I     R   R    A     A  D     D  C        O     O M     M
M     M     I     R    R   A     A  D     D  C     C  O     O M     M
M     M  IIIIIII  R     R  A     A  DDDDDD    CCCCC    OOOOO  M     M
```

= MISSILE RESEARCH AND DEVELOPMENT COMMAND =

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

MANUFACTURER: _____

COMPLETED BY: _____

TELEPHONE NO: _____

DATE: ____/____/____

GENERATION DATE: AUG 21,1979

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	_____
(2).	TESTER PART NUMBER (16 CHARACTERS)	_____
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	_____
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	_____

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GPOUP: T58 (GENERAL)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	____	____	____	____	____	____
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	____	____	____	____	____	____
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	____	____	____	____	____	____
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	____	____	____	____	____	____
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)						
(5).	TTL	____	____	____	____	____	____
(6).	CTL	____	____	____	____	____	____
(7).	RTL	____	____	____	____	____	____



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(8).	DTL						
(9).	IIL						
(10).	ECL						
(11).	DCTL						
(12).	RCTL						
(13).	HNIL						
(14).	CMOS						
(15).	NMOS						
(16).	PMOS						
(17).	EIA						
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC						
(19).	OTHER						
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)						
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)						
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)						
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)						
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)						
(2).	IF YES, CAPACITANCE RANGE MINIMUM						
(3).	CAPACITANCE RANGE MAXIMUM						

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)						
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)						
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)						
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)						
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)						

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)						
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?						

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)						
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)						
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)						
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)						
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)						
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)						
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)						
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)						
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)						

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)						
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..						
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICPOPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)

(4).	PIA						
(5).	ACIA						
(6).	PLA						
(7).	UART						
(8).	SAT						
(9).	SAR						
(10).	OTHER						
(11).	OTHER						
(12).	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART NUMBERS						
(13).							
(14).							
(15).							
(16)							

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)						
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)						
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

		SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)						
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)						

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	POLARITIES/VOLTAGE(S) MINIMUM						
(2).	POLARITIES/VOLTAGE(S) MAXIMUM						
(3).	ACCURACY						
(4).	MAXIMUM CURRENT DRAIN						
(5).	RIPPLE PEAK TO PEAK						
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)						
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)						
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(9).	INCREMENTAL RANGE MAXIMUM?						
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	CLOCK RATE MINIMUM						
(2).	CLOCK RATE MAXIMUM						
(3).	CLOCK PULSE WIDTH MINIMUM						
(4).	CLOCK PULSE WIDTH MAXIMUM						
(5).	CLOCK RISE TIME MINIMUM						
(6).	CLOCK RISE TIME MAXIMUM						
(7).	CLOCK FALL TIME MINIMUM						
(8).	CLOCK FALL TIME MAXIMUM						
(9).	CLOCK RESOLUTION						
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)						
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?						
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)						
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(14).	INCREMENTAL RANGE MAXIMUM?						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

*** DIGITAL TESTER QUESTIONNAIRE ***

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
	NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE						
(1).	TIME INTERVAL MINIMUM						
(2).	TIME INTERVAL MAXIMUM						
(3).	RISE TIME MINIMUM						
(4).	RISE TIME MAXIMUM						
(5).	FALL TIME MINIMUM						
(6).	FALL TIME MAXIMUM						
(7).	PULSE WIDTH RANGE MINIMUM						
(8).	PULSE WIDTH RANGE MAXIMUM						
(9).	VOLTAGE RANGE MINIMUM						
(10).	VOLTAGE RANGE MAXIMUM						
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)						
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(13).	INCREMENTAL RANGE MAXIMUM?						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	LOGIC LEVEL "1" MAXIMUM						
(2).	LOGIC LEVEL "1" MINIMUM						
(3).	LOGIC LEVEL "0" MAXIMUM						
(4).	LOGIC LEVEL "0" MINIMUM						
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..						
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(9).	INCREMENTAL RANGE MAXIMUM?						

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DATA BIT RATE MINIMUM						
(2).	DATA BIT RATE MAXIMUM						
(3).	WORD LENGTH MINIMUM						
(4).	WORD LENGTH MAXIMUM						
(5).	SEQUENCE LENGTH MINIMUM						
(6).	SEQUENCE LENGTH MAXIMUM						
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)						
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(11).	INCREMENTAL RANGE MAXIMUM?						

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	WORD RATE MINIMUM						
(2).	WORD RATE MAXIMUM						
(3).	WORD LENGTH MINIMUM						
(4).	WORD LENGTH MAXIMUM						
(5).	WORD SEQUENCE LENGTH MINIMUM						
(6).	WORD SEQUENCE LENGTH MAXIMUM						
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)						
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?						
(11).	INCREMENTAL RANGE MAXIMUM?						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
	NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.						
(1).	TIME INTERVAL MINIMUM	____	____	____	____	____	____
(2).	TIME INTERVAL MAXIMUM	____	____	____	____	____	____
(3).	RISE TIME MINIMUM	____	____	____	____	____	____
(4).	RISE TIME MAXIMUM	____	____	____	____	____	____
(5).	FALL TIME MINIMUM	____	____	____	____	____	____
(6).	FALL TIME MAXIMUM	____	____	____	____	____	____
(7).	PULSE WIDTH RANGE MINIMUM	____	____	____	____	____	____
(8).	PULSE WIDTH RANGE MAXIMUM	____	____	____	____	____	____
(9).	VOLTAGE RANGE MINIMUM	____	____	____	____	____	____
(10).	VOLTAGE RANGE MAXIMUM	____	____	____	____	____	____
(11).	IMPEDENCE	____	____	____	____	____	____
(12).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	____	____	____	____	____	____
(13).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	____	____	____	____	____	____

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	LOGIC LEVEL "1" MAXIMUM						
(2).	LOGIC LEVEL "1" MINIMUM						
(3).	LOGIC LEVEL "0" MAXIMUM						
(4).	LOGIC LEVEL "0" MINIMUM						
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	DATA BIT RATE MINIMUM						
(2).	DATA BIT RATE MAXIMUM						
(3).	WORD LENGTH MINIMUM						
(4).	WORD LENGTH MAXIMUM						
(5).	SEQUENCE LENGTH MINIMUM						
(6).	SEQUENCE LENGTH MAXIMUM						
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL TESTER QUESTIONNAIRE * * *

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4	SET # 5	SET # 6
(1).	WORD RATE MINIMUM						
(2).	WORD RATE MAXIMUM						
(3).	WORD LENGTH MINIMUM						
(4).	WORD LENGTH MAXIMUM						
(5).	WORD SEQUENCE LENGTH MINIMUM						
(6).	WORD SEQUENCE LENGTH MAXIMUM						
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)						
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?						

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB GROUP P80 WILL BE MATCHED TO T75.

SECTION IIB
D/PCB TESTER CAPABILITY SUMMARY

```
MM    MM  IIIIIII  RRRRRR    AAAAA   DDDDDD    CCCCC    OOOOO   M     M
MM   MM     I     R     R  A     A  D     D  C     C  O     O  MM   MM
M M M M     I     R     R  A     A  D     D  C        O     O  M M M M
M  M  M     I     RRRRRR   AAAAAAA  D     D  C        O     O  M  M  M
M     M     I     R   R    A     A  D     D  C        O     O  M     M
M     M     I     R    R   A     A  D     D  C     C  O     O  M     M
M     M  IIIIIII  R     R  A     A  DDDDDD    CCCCC    OOOOO   M     M
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= MISSILE RESEARCH AND DEVELOPMENT COMMAND =

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

DIGITAL PCB TESTER CAPABILITY SUMMARY

(TABULATION BY TESTER)

AUG 21,1979

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	FUNCTIONAL BOARD TEST SYSTEM
(2).	TESTER PART NUMBER (16 CHARACTERS)	L135
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	TERADYNE, INC.
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	TERADYNE

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.456000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.456000E+03

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	0.456000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.200000E+01
(12).	RCTL	0.200000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.0
(3).	CAPACITANCE RANGE MAXIMUM	0.0

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.999000E+03

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.0

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

DESCRIPTION	SET # 1
CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4). PIA	0.200000E+01
(5). ACIA	0.200000E+01
(6). PLA	0.200000E+01
(7). UART	0.200000E+01
(8). SAT	0.200000E+01
(9). SAR	0.200000E+01
(10). OTHER	0.100000E+01
(11). OTHER	0.100000E+01
IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART	
(12). NUMBERS	0.0
(13).	0.0
(14).	0.0
(15).	0.0
(16).	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S) MINIMUM	-.600000E+01	-.160000E+02	-.500000E+02
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.600000E+01	0.160000E+02	0.500000E+02
(3).	ACCURACY	0.250000E+00	0.250000E+00	0.250000E+00
(4).	MAXIMUM CURRENT DRAIN	0.600000E+01	0.160000E+01	0.0
(5).	RIPPLE PEAK TO PEAK	0.500000E-02	0.500000E-02	0.500000E-02
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.100000E+01	0.100000E+01	0.100000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.0	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0	0.0
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,P=2)	0.100000E+01	0.100000E+01	0.100000E+01

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2
(1).	CLOCK RATE MINIMUM	0.250000E+02	0.100000E+03
(2).	CLOCK RATE MAXIMUM	0.160000E+05	0.500000E+07
(3).	CLOCK PULSE WIDTH MINIMUM	0.300000E-06	0.200000E-07
(4).	CLOCK PULSE WIDTH MAXIMUM	0.390000E-01	0.400000E-05
(5).	CLOCK RISE TIME MINIMUM	0.0	0.500000E-08
(6).	CLOCK RISE TIME MAXIMUM	0.0	0.100000E-07
(7).	CLOCK FALL TIME MINIMUM	0.0	0.500000E-08
(8).	CLOCK FALL TIME MAXIMUM	0.0	0.100000E-07
(9).	CLOCK RESOLUTION	0.100000E-07	0.100000E-08
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.0	0.0
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.100000E+01	0.100000E+01
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-07	0.100000E-07
(14).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.160000E+02	0.160000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.160000E+02	-.160000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.600000E+01	0.600000E+01
(4).	LOGIC LEVEL "0" MINIMUM	-.600000E+01	-.600000E+01
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.0
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.0
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01	0.0
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-01	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+04
(2).	DATA BIT RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.180000E+02
(4).	WORD LENGTH MAXIMUM	0.400000E+04
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.432000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+04
(2).	WORD RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.400000E+04
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.200000E-07
(2). TIME INTERVAL MAXIMUM	0.107000E+03
(3). RISE TIME MINIMUM	0.100000E-06
(4). RISE TIME MAXIMUM	0.107000E+03
(5). FALL TIME MINIMUM	0.100000E-06
(6). FALL TIME MAXIMUM	0.107000E+03
(7). PULSE WIDTH RANGE MINIMUM	0.200000E-07
(8). PULSE WIDTH RANGE MAXIMUM	0.107000E+03
(9). VOLTAGE RANGE MINIMUM	-.160000E+02
(10). VOLTAGE RANGE MAXIMUM	0.160000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.160000E+02	0.160000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.160000E+02	-.160000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.160000E+02	0.160000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.160000E+02	-.160000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.0
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.0

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+01
(2).	DATA BIT RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.0
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+01
(2).	WORD RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.456000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION SET # 1

GROUP P80 WILL BE MATCHED TO T75.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	AUTOMATIC LOGIC BOARD TESTER
(2).	TESTER PART NUMBER (16 CHARACTERS)	TL-8
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	TRACE INSTRUMENTS

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.256000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.256000E+03

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT	
(3).	DIGITAL SIGNALS	0.256000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.200000E+01
(12).	RCTL	0.200000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.200000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.100000E-11
(3).	CAPACITANCE RANGE MAXIMUM	0.0

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.100000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.100000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.990000E+09

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.655360E+05

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.655360E+05
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.655360E+05
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.655360E+05

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E+01
(9).	SAR	0.200000E+01
(10).	OTHER	0.200000E+01
(11).	OTHER	0.200000E+01
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART NUMBERS	
(12).		0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0	0.0	-.200000E+02	-.200000E+02
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.500000E+01	0.150000E+01	0.200000E+02	0.200000E+02
(3).	ACCURACY	0.500000E-01	0.500000E-01	0.500000E-01	0.500000E-01
(4).	MAXIMUM CURRENT DRAIN	0.500000E+01	0.200000E+01	0.0	0.0
(5).	RIPPLE PEAK TO PEAK	0.100000E+00	0.100000E+00	0.100000E+00	0.100000E+00
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.100000E+01	0.200000E+01	0.100000E+01	0.100000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.100000E+01	0.200000E+01	0.0	0.0



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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3	SET # 4
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.200000E-01	0.0	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.200000E+02	0.0	0.0
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.100000E+01	0.100000E+01	0.0	0.0

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.0
(2).	CLOCK RATE MAXIMUM	0.200000E+08
(3).	CLOCK PULSE WIDTH MINIMUM	0.300000E-07
(4).	CLOCK PULSE WIDTH MAXIMUM	0.300000E-07
(5).	CLOCK RISE TIME MINIMUM	0.500000E-08
(6).	CLOCK RISE TIME MAXIMUM	0.250000E-07
(7).	CLOCK FALL TIME MINIMUM	0.120000E-07
(8).	CLOCK FALL TIME MAXIMUM	0.120000E-07
(9).	CLOCK RESOLUTION	0.500000E-02
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.200000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.800000E+01
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01



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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.300000E+03
(14).	INCREMENTAL RANGE MAXIMUM?	0.200000E+08

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
	NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE	
(1).	TIME INTERVAL MINIMUM	0.500000E-07
(2).	TIME INTERVAL MAXIMUM	0.350000E+01
(3).	RISE TIME MINIMUM	0.0
(4).	RISE TIME MAXIMUM	0.500000E+00
(5).	FALL TIME MINIMUM	0.0
(6).	FALL TIME MAXIMUM	0.500000E+00
(7).	PULSE WIDTH RANGE MINIMUM	0.500000E-07
(8).	PULSE WIDTH RANGE MAXIMUM	0.300000E+01
(9).	VOLTAGE RANGE MINIMUM	0.200000E-01
(10).	VOLTAGE RANGE MAXIMUM	0.200000E+02
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.500000E-07
(13).	INCREMENTAL RANGE MAXIMUM?	0.300000E+01

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.150000E+02	0.200000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E-01	-.200000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.0	0.200000E+02
(4).	LOGIC LEVEL "0" MINIMUM	0.0	-.200000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.256000E+03	0.0
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01	0.0
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.200000E-01	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.200000E+02	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.500000E-06
(2).	DATA BIT RATE MAXIMUM	0.990000E+08
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.655360E+05
(5).	SEQUENCE LENGTH MINIMUM	0.100000E+01
(6).	SEQUENCE LENGTH MAXIMUM	0.990000E+08
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.256000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(11).	INCREMENTAL RANGE MAXIMUM?	0.655360E+05

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.500000E-06
(2).	WORD RATE MAXIMUM	0.655260E+05
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.655260E+05
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.256000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(11).	INCREMENTAL RANGE MAXIMUM?	0.655260E+05

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.500000E-07
(2). TIME INTERVAL MAXIMUM	0.990000E+08
(3). RISE TIME MINIMUM	0.0
(4). RISE TIME MAXIMUM	0.0
(5). FALL TIME MINIMUM	0.0
(6). FALL TIME MAXIMUM	0.0
(7). PULSE WIDTH RANGE MINIMUM	0.500000E-07
(8). PULSE WIDTH RANGE MAXIMUM	0.350000E+01
(9). VOLTAGE RANGE MINIMUM	0.200000E-01
(10). VOLTAGE RANGE MAXIMUM	0.200000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.200000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.200000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.200000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.200000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.256000E+03

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
1).	DATA BIT RATE MINIMUM	0.0
2).	DATA BIT RATE MAXIMUM	0.571000E+06
3).	[illegible] MINIMUM	0.100000E+01
4).	[illegible] MAXIMUM	0.990000E+08
5).	[illegible] MINIMUM	0.100000E+01
6).	[illegible] MAXIMUM	0.655260E+05
7).	[illegible] CAPABILITY? (NO=1,YES=2)	0.200000E+01
8).	[illegible] AVAILABLE SIMULTANEOUSLY?	0.256000E+03

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
(1). WORD RATE MINIMUM	0.0
(2). WORD RATE MAXIMUM	0.2000000E+07
(3). WORD LENGTH MINIMUM	0.1000000E+01
(4). WORD LENGTH MAXIMUM	0.3200000E+02
(5). WORD SEQUENCE LENGTH MINIMUM	0.0
(6). WORD SEQUENCE LENGTH MAXIMUM	0.0
(7). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.256000E+03

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

GROUP P80 WILL BE MATCHED TO T75.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	DTS-70 DIGITAL TEST SYSTEM
(2).	TESTER PART NUMBER (16 CHARACTERS)	9571A
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	HEWLETT PACKARD CO.

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.360000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.360000E+03

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	0.360000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.100000E+01
(11).	DCTL	0.200000E+01
(12).	RCTL	0.200000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.200000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.100000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.0
(3).	CAPACITANCE RANGE MAXIMUM	0.999000E+03

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1 YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.100000E+03

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.999000E+03

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.819200E+04
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.819200E+04
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME?	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E+01
(9).	SAR	0.200000E+01
(10).	OTHER	0.200000E+01
(11).	OTHER	0.200000E+01
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART NUMBERS	
(12).		0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0	-.250000E+02	0.0
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.250000E+02	0.0	0.200000E+02
(3).	ACCURACY	0.150000E+01	0.150000E+01	0.150000E+01
(4).	MAXIMUM CURRENT DRAIN	0.200000E+01	0.200000E+01	0.0
(5).	RIPPLE PEAK TO PEAK	0.0	0.0	0.200000E+01
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.200000E+01	0.200000E+01	0.200000E+02

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-01	0.100000E-01	0.200000E+01
(9).	INCREMENTAL RANGE MAXIMUM?	0.250000E+02	0.250000E+02	-.123443E+04
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.200000E+01	0.200000E+01	0.0

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.100000E-01
(2).	CLOCK RATE MAXIMUM	0.500000E+07
(3).	CLOCK PULSE WIDTH MINIMUM	0.100000E-05
(4).	CLOCK PULSE WIDTH MAXIMUM	0.100000E+03
(5).	CLOCK RISE TIME MINIMUM	0.0
(6).	CLOCK RISE TIME MAXIMUM	0.0
(7).	CLOCK FALL TIME MINIMUM	0.0
(8).	CLOCK FALL TIME MAXIMUM	0.0
(9).	CLOCK RESOLUTION	0.100000E-06
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.100000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.100000E+01
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-01
(14).	INCREMENTAL RANGE MAXIMUM?	0.500000E+07

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.150000E+02	0.160000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.200000E+01	0.350000E+01	-.160000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.800000E+00	0.100000E+01	0.160000E+02
(4).	LOGIC LEVEL "0" MINIMUM	0 0	0.0	-.160000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.200000E+01	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.600000E+01	0.600000E+01	0.600000E+01
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.100000E+01	0.100000E+01	0.200000E+01
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.0	-.160000E+02
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0	0.160000E+02

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

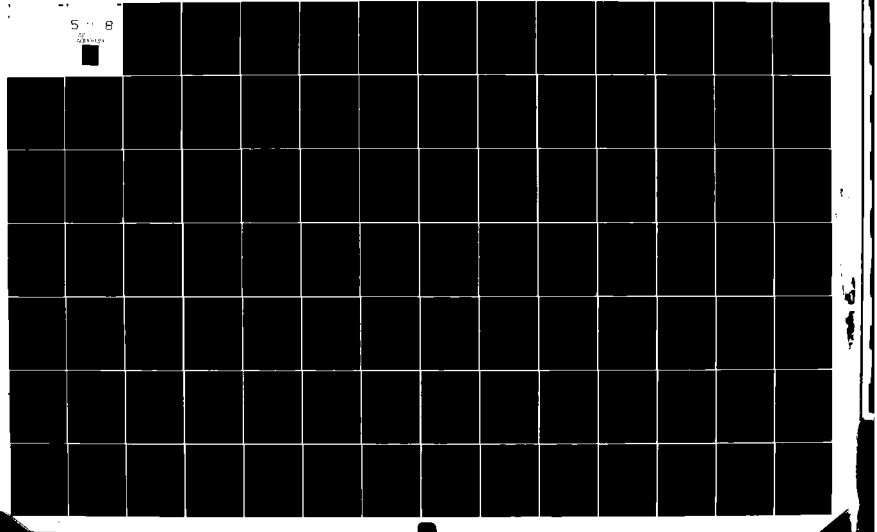
* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.100000E-06
(2). TIME INTERVAL MAXIMUM	0.500000E-01
(3). RISE TIME MINIMUM	0.0
(4). RISE TIME MAXIMUM	0.0
(5). FALL TIME MINIMUM	0.0
(6). FALL TIME MAXIMUM	0.0
(7). PULSE WIDTH RANGE MINIMUM	0.100000E-06
(8). PULSE WIDTH RANGE MAXIMUM	0.500000E-04
(9). VOLTAGE RANGE MINIMUM	-.300000E+02
(10). VOLTAGE RANGE MAXIMUM	0.300000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	LOGIC LEVEL "1" MAXIMUM	0.500000E+01	0.150000E+02	0.160000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.240000E+01	0.700000E+00	-.160000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.500000E+00	0.500000E+00	0.160000E+02
(4).	LOGIC LEVEL "0" MINIMUM	0.0	0.0	-.160000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.200000E+01	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.600000E+01	0.600000E+01	0.600000E+01



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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	CAPABLE
(2).	TESTER PART NUMBER (16 CHARACTERS)	4000
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	COMPUTER AUTOMATION

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.102300E+04
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.102300E+04

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	0.102300E+04
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.0
(3).	CAPACITANCE RANGE MAXIMUM	0.999000E+03

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

P P I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.999000E+03

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.999000E+03

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMAR: * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.999900E+04
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.999990E+05
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.409600E+04

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E 1
(9).	SAR	0.200000E+01
(10).	OTHER	0.200000E+01
(11).	OTHER	0.200000E+01
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART	
(12).	NUMBERS	0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.100000E+02
(3).	ACCURACY	0.300000E-01
(4).	MAXIMUM CURRENT DRAIN	0.130000E+02
(5).	RIPPLE PEAK TO PEAK	0.0
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-01
(9).	INCREMENTAL RANGE MAXIMUM?	0.100000E+02
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.200000E+01

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.100000E+04
(2).	CLOCK RATE MAXIMUM	0.200000E+08
(3).	CLOCK PULSE WIDTH MINIMUM	0.250000E-07
(4).	CLOCK PULSE WIDTH MAXIMUM	0.500000E+05
(5).	CLOCK RISE TIME MINIMUM	0.100000E-07
(6).	CLOCK RISE TIME MAXIMUM	0.200000E-07
(7).	CLOCK FALL TIME MINIMUM	0.100000E-07
(8).	CLOCK FALL TIME MAXIMUM	0.200000E-07
(9).	CLOCK RESOLUTION	0.250000E-07
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.200000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.800000E+01
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.250000E-07
(14).	INCREMENTAL RANGE MAXIMUM?	0.500000E-03

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
	NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE	
(1).	TIME INTERVAL MINIMUM	0.0
(2).	TIME INTERVAL MAXIMUM	0.0
(3).	RISE TIME MINIMUM	0.100000E-07
(4).	RISE TIME MAXIMUM	0.200000E-07
(5).	FALL TIME MINIMUM	0.100000E-07
(6).	FALL TIME MAXIMUM	0.200000E-07
(7).	PULSE WIDTH RANGE MINIMUM	0.250000E-07
(8).	PULSE WIDTH RANGE MAXIMUM	0.500000E-03
(9).	VOLTAGE RANGE MINIMUM	-.180000E+02
(10).	VOLTAGE RANGE MAXIMUM	0.180000E+02
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.250000E-07
(13).	INCREMENTAL RANGE MAXIMUM?	0.500000E-03

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.180000E+02	0.180000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.180000E+02	-.180000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.180000E+02	0.180000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.180000E+02	-.180000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.200000E+01
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01	0.200000E+01
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E-01	0.100000E-01
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+04
(2).	DATA BIT RATE MAXIMUM	0.200000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.400000E+04
(5).	SEQUENCE LENGTH MINIMUM	0.100000E+01
(6).	SEQUENCE LENGTH MAXIMUM	0.400000E+04
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.512000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+04
(11).	INCREMENTAL RANGE MAXIMUM?	0.200000E+07

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+04
(2).	WORD RATE MAXIMUM	0.200000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.512000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.512000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+04
(11).	INCREMENTAL RANGE MAXIMUM?	0.200000E+07

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.0
(2). TIME INTERVAL MAXIMUM	0.0
(3). RISE TIME MINIMUM	0.0
(4). RISE TIME MAXIMUM	0.0
(5). FALL TIME MINIMUM	0.0
(6). FALL TIME MAXIMUM	0.0
(7). PULSE WIDTH RANGE MINIMUM	0.250000E-07
(8). PULSE WIDTH RANGE MAXIMUM	0.350000E+01
(9). VOLTAGE RANGE MINIMUM	-.200000E+02
(10). VOLTAGE RANGE MAXIMUM	0.200000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.512000E+03

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.200000E+02	0.200000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.200000E+02	-.200000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.200000E+02	0.200000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.200000E+02	-.200000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.0
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.0

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHAPACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+04
(2).	DATA BIT RATE MAXIMUM	0.200000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.400000E+04
(5).	SEQUENCE LENGTH MINIMUM	0.100000E+01
(6).	SEQUENCE LENGTH MAXIMUM	0.400000E+04
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.512000E+03

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+04
(2).	WORD RATE MAXIMUM	0.200000E+07
(3).	WORD LENGTH MINIMUM	0.100000E+01
(4).	WORD LENGTH MAXIMUM	0.512000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.512000E+03

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB



PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1
GROUP P80 WILL BE MATCHED TO T75.	

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	LOGIC TEST SYSTEM
(2).	TESTER PART NUMBER (16 CHARACTERS)	1795 - HD/FD
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	GEN RAD, INC.

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1	SET # 2
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.240000E+03	0.480000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.240000E+03	0.480000E+03

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

*** DIGITAL PCB TESTER CAPABILITY SUMMARY ***

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT		
(3).	DIGITAL SIGNALS	0.240000E+03	0.480000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01	0.0
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)		
(5).	TTL	0.200000E+01	0.0
(6).	CTL	0.100000E+01	0.0
(7).	RTL	0.200000E+01	0.0
(8).	DTL	0.200000E+01	0.0
(9).	IIL	0.200000E+01	0.0
(10).	ECL	0.200000E+01	0.0
(11).	DCTL	0.100000E+01	0.0
(12).	RCTL	0.100000E+01	0.0
(13).	HNIL	0.100000E+01	0.0
(14).	CMOS	0.200000E+01	0.0
(15).	NMOS	0.200000E+01	0.0
(16).	PMOS	0.200000E+01	0.0
(17).	EIA	0.100000E+01	0.0
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.200000E+01	0.0
(19).	OTHER	0.100000E+01	0.0
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01	0.0
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01	0.0

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01	0.0
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01	0.0
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.100000E+01	0.0

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.999900E+04

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.999900E+04

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.450000E+05
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.400000E+04
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME?	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E+01
(9).	SAR	0.200000E+01
(10).	OTHER	0.200000E+01
(11).	OTHER	0.200000E+01
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART NUMBERS	
(12).		0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.700000E+01
(3).	ACCURACY	0.100000E+01
(4).	MAXIMUM CURRENT DRAIN	0.100000E+02
(5).	RIPPLE PEAK TO PEAK	0.0
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.100000E+01

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.100000E+01

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.0
(2).	CLOCK RATE MAXIMUM	0.660000E+05
(3).	CLOCK PULSE WIDTH MINIMUM	0.0
(4).	CLOCK PULSE WIDTH MAXIMUM	0.0
(5).	CLOCK RISE TIME MINIMUM	0.0
(6).	CLOCK RISE TIME MAXIMUM	0.0
(7).	CLOCK FALL TIME MINIMUM	0.0
(8).	CLOCK FALL TIME MAXIMUM	0.0
(9).	CLOCK RESOLUTION	0.0
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.0
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.0
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.100000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(14).	INCREMENTAL RANGE MAXIMUM?	0.0

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.150000E+02	0.120000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.150000E+02	0.100000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.150000E+02	0.700000E+00
(4).	LOGIC LEVEL "0" MINIMUM	-.150000E+02	0.0
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.100000E+01	0.100000E+01
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01	0.200000E+01
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.730000E-02	0.730000E-02
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.0
(2).	DATA BIT RATE MAXIMUM	0.660000E+05
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.480000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.800000E+04
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.100000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.0
(2).	WORD RATE MAXIMUM	0.660000E+05
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.480000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.100000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.120000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.0
(3).	LOGIC LEVEL "0" MAXIMUM	0.130000E+01
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.0
(2).	DATA BIT RATE MAXIMUM	0.660000E+05
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.480000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.400000E+04
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.0
(2).	WORD RATE MAXIMUM	0.660000E+05
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.480000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.480000E+03

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

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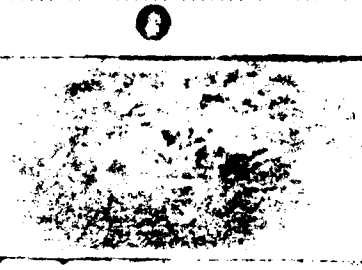
* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

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PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION SET # 1

GROUP P80 WILL BE MATCHED TO T75.



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(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	TEXAS INSTRUMENTS ATS-960
(2).	TESTER PART NUMBER (16 CHARACTERS)	ATS-960
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	TEXAS INSTRUMENTS

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.512000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.256000E+03

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(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	0.256000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.200000E+01
(12).	RCTL	0.200000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.200000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01



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(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.100000E-11
(3).	CAPACITANCE RANGE MAXIMUM	0.100000E-03

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

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(TABULATION BY TESTER)

PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.100000E+01

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.100000E+09

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.256000E+06
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.256000E+06
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.0

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

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(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.100000E+01
(5).	ACIA	0.100000E+01
(6).	PLA	0.100000E+01
(7).	UART	0.100000E+01
(8).	SAT	0.100000E+01
(9).	SAR	0.100000E+01
(10).	OTHER	0.100000E+01
(11).	OTHER	0.0
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART	
(12).	NUMBERS	0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0

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(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTEP FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0	0.0
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.600000E+03	0.600000E+03
(3).	ACCURACY	0.100000E-01	0.100000E-01
(4).	MAXIMUM CURRENT DRAIN	0.120000E+02	0.120000E+02
(5).	RIPPLE PEAK TO PEAK	0.0	0.0
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.100000E+01	0.100000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.100000E+01	0.200000E+01

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.100000E+02
(2).	CLOCK RATE MAXIMUM	0.500000E+08
(3).	CLOCK PULSE WIDTH MINIMUM	0.100000E-07
(4).	CLOCK PULSE WIDTH MAXIMUM	0.100000E-04
(5).	CLOCK RISE TIME MINIMUM	0.500000E-08
(6).	CLOCK RISE TIME MAXIMUM	0.100000E-04
(7).	CLOCK FALL TIME MINIMUM	0.500000E-08
(8).	CLOCK FALL TIME MAXIMUM	0.100000E-04
(9).	CLOCK RESOLUTION	0.100000E+00
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.200000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.200000E+02
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+00
(14).	INCREMENTAL RANGE MAXIMUM?	0.100000E+06

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
	NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE	
(1).	TIME INTERVAL MINIMUM	0.100000E-06
(2).	TIME INTERVAL MAXIMUM	0.100000E-03
(3).	RISE TIME MINIMUM	0.500000E-08
(4).	RISE TIME MAXIMUM	0.100000E-04
(5).	FALL TIME MINIMUM	0.500000E-08
(6).	FALL TIME MAXIMUM	0.100000E-04
(7).	PULSE WIDTH RANGE MINIMUM	0.100000E-07
(8).	PULSE WIDTH RANGE MAXIMUM	0.100000E-01
(9).	VOLTAGE RANGE MINIMUM	0.500000E+00
(10).	VOLTAGE RANGE MAXIMUM	0.100000E+02
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(13).	INCREMENTAL RANGE MAXIMUM?	0.0

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.150000E+02	0.150000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.150000E+02	-.150000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.150000E+02	0.150000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.150000E+02	-.150000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.0
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.0
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01	0.0
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.125000E-01	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.125000E-01	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+01
(2).	DATA BIT RATE MAXIMUM	0.100000E+08
(3).	WORD LENGTH MINIMUM	0.160000E+02
(4).	WORD LENGTH MAXIMUM	0.256000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.100000E+01
(6).	SEQUENCE LENGTH MAXIMUM	0.320000E+05
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(11).	INCREMENTAL RANGE MAXIMUM?	0.166000E+06

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+01
(2).	WORD RATE MAXIMUM	0.166000E+06
(3).	WORD LENGTH MINIMUM	0.160000E+02
(4).	WORD LENGTH MAXIMUM	0.256000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(11).	INCREMENTAL RANGE MAXIMUM?	0.100000E+04

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

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(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.150000E-09
(2). TIME INTERVAL MAXIMUM	0.100000E+02
(3). RISE TIME MINIMUM	0.150000E-09
(4). RISE TIME MAXIMUM	0.100000E+02
(5). FALL TIME MINIMUM	0.150000E-09
(6). FALL TIME MAXIMUM	0.100000E+02
(7). PULSE WIDTH RANGE MINIMUM	0.150000E-09
(8). PULSE WIDTH RANGE MAXIMUM	0.100000E+02
(9). VOLTAGE RANGE MINIMUM	0.300000E+00
(10). VOLTAGE RANGE MAXIMUM	0.300000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.100000E+02

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTEP)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1	SET # 2
(1).	LOGIC LEVEL "1" MAXIMUM	0.150000E+02	0.150000E+02
(2).	LOGIC LEVEL "1" MINIMUM	-.150000E+02	-.150000E+02
(3).	LOGIC LEVEL "0" MAXIMUM	0.150000E+02	0.150000E+02
(4).	LOGIC LEVEL "0" MINIMUM	-.150000E+02	-.150000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01	0.0
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.200000E+01	0.0

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+01
(2).	DATA BIT RATE MAXIMUM	0.100000E+08
(3).	WORD LENGTH MINIMUM	0.160000E+02
(4).	WORD LENGTH MAXIMUM	0.256000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.100000E+01
(6).	SEQUENCE LENGTH MAXIMUM	0.320000E+05
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

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(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+01
(2).	WORD RATE MAXIMUM	0.166000E+06
(3).	WORD LENGTH MINIMUM	0.160000E+02
(4).	WORD LENGTH MAXIMUM	0.256000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

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PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION SET # 1

GROUP P80 WILL BE MATCHED TO T75.

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(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	LOGIC TESTER
(2).	TESTER PART NUMBER (16 CHARACTERS)	3040 A
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	JOHN FLUKE MFG. CO.

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.240000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.240000E+03

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

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(TABULATION BY TESTER)

PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT	
(3).	DIGITAL SIGNALS	0.240000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.200000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.100000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.200000E+01
(12).	RCTL	0.200000E+01
(13).	HNIL	0.200000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.100000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01



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PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T59 (CAPACITORS IN LOGIC PATH)

	DESCRIPTION	SET # 1
(1).	CAN TESTER TEST UUT WITH CAPACITORS IN LOGIC PATH? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, CAPACITANCE RANGE MINIMUM	0.100000E-09
(3).	CAPACITANCE RANGE MAXIMUM	0.100000E-03

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1

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PARAMETER GROUP: T60 (LOOPS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T6I (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.100000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.100000E+02

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.100000E+07

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS) - CONTINUED -

	DESCRIPTION	SET # 1
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.914000E+09
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.457000E+09
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.457000E+09

PARAMETER GROUP: T65 (MICROPROCESSORS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME? ..	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0

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PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E+01
(9).	SAR	0.200000E+01
(10).	OTHER	0.200000E+01
(11).	OTHER	0.0
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART	
(12).	NUMBERS	0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0

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(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0	0.0	-.150000E+02
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.500000E+01	0.150000E+02	0.0
(3).	ACCURACY	0.300000E+01	0.100000E+01	0.100000E+01
(4).	MAXIMUM CURRENT DRAIN	0.500000E+01	0.100000E+01	0.100000E+01
(5).	RIPPLE PEAK TO PEAK	0.150000E+00	0.250000E+00	0.250000E+00
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01	0.200000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.200000E+01	0.200000E+01	0.200000E+01

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PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.300000E+01	0.300000E+01	0.300000E+01
(9).	INCREMENTAL RANGE MAXIMUM?	0.150000E+02	0.150000E+02	0.150000E+02
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.200000E+01	0.200000E+01	0.200000E+01

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1
(1).	CLOCK RATE MINIMUM	0.100000E+01
(2).	CLOCK RATE MAXIMUM	0.500000E+07
(3).	CLOCK PULSE WIDTH MINIMUM	0.160000E-05
(4).	CLOCK PULSE WIDTH MAXIMUM	0.800000E+01
(5).	CLOCK RISE TIME MINIMUM	0.0
(6).	CLOCK RISE TIME MAXIMUM	0.0
(7).	CLOCK FALL TIME MINIMUM	0.0
(8).	CLOCK FALL TIME MAXIMUM	0.0
(9).	CLOCK RESOLUTION	0.200000E-06
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.200000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.240000E+02
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.200000E+04
(14).	INCREMENTAL RANGE MAXIMUM?	0.0

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
	NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE	
(1).	TIME INTERVAL MINIMUM	0.100000E+01
(2).	TIME INTERVAL MAXIMUM	0.500000E+07
(3).	RISE TIME MINIMUM	0.300000E-07
(4).	RISE TIME MAXIMUM	0.0
(5).	FALL TIME MINIMUM	0.300000E-07
(6).	FALL TIME MAXIMUM	0.0
(7).	PULSE WIDTH RANGE MINIMUM	0.200000E-06
(8).	PULSE WIDTH RANGE MAXIMUM	0.100000E+01
(9).	VOLTAGE RANGE MINIMUM	-.150000E+02
(10).	VOLTAGE RANGE MAXIMUM	0.150000E+02
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01

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PARAMETER GROUP: T09 (GENERAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(13).	INCREMENTAL RANGE MAXIMUM?	0.500000E+07

T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.135000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.325000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.500000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.100000E+01
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.300000E+01
(9).	INCREMENTAL RANGE MAXIMUM?	0.150000E+02

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+01
(2).	DATA BIT RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.240000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.400000E+08
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.240000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.100000E+01
(11).	INCREMENTAL RANGE MAXIMUM?	0.500000E+07

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+01
(2).	WORD RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.400000E+08
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.240000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.400000E+08

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.100000E+01
(2). TIME INTERVAL MAXIMUM	0.200000E-06
(3). RISE TIME MINIMUM	0.300000E-07
(4). RISE TIME MAXIMUM	0.0
(5). FALL TIME MINIMUM	0.300000E-07
(6). FALL TIME MAXIMUM	0.0
(7). PULSE WIDTH RANGE MINIMUM	0.100000E+01
(8). PULSE WIDTH RANGE MAXIMUM	0.200000E-06
(9). VOLTAGE RANGE MINIMUM	0.300000E+01
(10). VOLTAGE RANGE MAXIMUM	0.150000E+02
(11). IMPEDENCE	0.0
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.240000E+03

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.135000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.325000E+01
(3).	LOGIC LEVEL "0" MAXIMUM	0.500000E+00
(4).	LOGIC LEVEL "0" MINIMUM	0.0
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.100000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.100000E+01

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.100000E+01
(2).	DATA BIT RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.400000E+08
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.400000E+08
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.240000E+03

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.100000E+01
(2).	WORD RATE MAXIMUM	0.500000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.400000E+08
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.240000E+03

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

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PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

GROUP P80 WILL BE MATCHED TO T75.

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(TABULATION BY TESTER)

DIGITAL TESTER FEATURES

PARAMETER GROUP: T57 (TESTER IDENTIFICATION)

	DESCRIPTION	VALUE
(1).	TESTER NOMENCLATURE (32 CHARACTERS)	DYNAMIC DIGITAL TEST SYSYEM
(2).	TESTER PART NUMBER (16 CHARACTERS)	1796 A
(3).	TESTER NATIONAL STOCK NUMBER (16 CHARACTERS)	
(4).	TESTER MANUFACTURER NAME (20 CHARACTERS) ..	GEN RAD

NOTE: IF THERE IS MORE THAN 1 SET OF A PARAMETER GROUP SO INDICATE BY ENTRIES THROUGHOUT. ALSO INDICATE UNITS OF ALL PARAMETERS.

PARAMETER GROUP: T58 (GENERAL)

	DESCRIPTION	SET # 1
(1).	WHAT IS THE MAXIMUM NUMBER OF I/O PINS THE TESTER CAN PROVIDE?	0.216000E+03
(2).	NUMBER OF I/O PINS WHICH IS DESIGNATED FOR DIGITAL INPUTS	0.216000E+03

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PARAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(3).	NUMBER OF I/O PINS WHICH IS DESIGNATED TO MEASURE OUTPUT DIGITAL SIGNALS	0.216000E+03
(4).	CAN TESTER DIRECTLY TEST TRI-STATE LOGIC? (NO=1,YES=2)	0.200000E+01
	INDICATE ALL LOGIC FAMILIES THAT CAN BE DIRECTLY TESTED BY THE TESTER (NO=1,YES=2)	
(5).	TTL	0.200000E+01
(6).	CTL	0.100000E+01
(7).	RTL	0.200000E+01
(8).	DTL	0.200000E+01
(9).	IIL	0.200000E+01
(10).	ECL	0.200000E+01
(11).	DCTL	0.100000E+01
(12).	RCTL	0.100000E+01
(13).	HNIL	0.100000E+01
(14).	CMOS	0.200000E+01
(15).	NMOS	0.200000E+01
(16).	PMOS	0.200000E+01
(17).	EIA	0.100000E+01
(18).	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC	0.200000E+01
(19).	OTHER	0.100000E+01
(20).	CAN TESTER TEST SSI? (NO=1,YES=2)	0.200000E+01
(21).	CAN TESTER TEST MSI? (NO=1,YES=2)	0.200000E+01

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PAPAMETER GROUP: T58 (GENERAL) - CONTINUED -

	DESCRIPTION	SET # 1
(22).	CAN TESTER TEST LSI WITH 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(23).	CAN TESTER TEST LSI WITH MORE THAN 24 PINS/PACKAGE? (NO=1,YES=2)	0.200000E+01
(24).	CAN TESTER TEST DYNAMIC IC'S? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T60 (LOOPS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE SYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST THE UUT WITH THE SYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ASYNCHRONOUS UNBROKEN OR UNINTERRUPTED FEEDBACK LOOPS? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER TEST THE UUT WITH THE ASYNCHRONOUS FEEDBACK LOOPS BROKEN OR INTERRUPTED? (NO=1,YES=2)	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T61 (WIRED AND (BUSES))

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE LARGE FAN-IN (WIRED-AND) CONNECTIONS? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER TEST BIDIRECTIONAL BUSES? (NO=1,YES=2)	0.200000E+01

PARAMETER GROUP: T62 (ONE-SHOTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE ONE-SHOT DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM DELAY THE TESTER CAN TEST?	0.900000E+10

PARAMETER GROUP: T63 (COUNTERS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE COUNTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MAXIMUM COUNT THAT THE TESTER CAN TEST? (EXPRESS DECIMALLY)	0.900000E+10

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T64 (STORAGE ELEMENTS)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE FLIP-FLOP DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE REGISTERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE ROM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE ROM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.450000E+05
(5).	CAN TESTER FAULT ISOLATE RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(6).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.400000E+04
(7).	CAN TESTER FAULT ISOLATE DYNAMIC RAM HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(8).	IF YES, WHAT IS THE MAXIMUM SIZE OF THE DYNAMIC RAM THAT THE TESTER CAN TEST? (EXPRESS IN BITS)	0.400000E+04

PARAMETER GROUP: T65 (MICROPROCESSORS)

DESCRIPTION	SET # 1

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(TABULATION BY TESTER)

PARAMETER GROUP: T65 (MICROPROCESSORS) - CONTINUED -

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE MICROPROCESSORS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	IF YES, WHAT IS THE MICROPROCESSOR MANUFACTURER'S NAME?	0.0
(3).	WHAT IS THE MANUFACTURER'S MICROPROCESSOR PART/MODEL NUMBER?	0.0
	CAN THE TESTER FAULT ISOLATE THE FOLLOWING MICROPROCESSOR SUPPORT CHIPS? (NO=1,YES=2)	
(4).	PIA	0.200000E+01
(5).	ACIA	0.200000E+01
(6).	PLA	0.200000E+01
(7).	UART	0.200000E+01
(8).	SAT	0.200000E+01
(9).	SAR	0.200000E+01
(10).	OTHER	0.0
(11).	OTHER	0.0
	IF YES, LIST THE SUPPORT CHIPS MANUFACTURERS AND PART	
(12).	NUMBERS	0.0
(13).		0.0
(14).		0.0
(15).		0.0
(16).		0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T66 (COMBINATORIAL DEVICES)

	DESCRIPTION	SET # 1
(1).	CAN TESTER FAULT ISOLATE DECODER/DEMULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(2).	CAN TESTER FAULT ISOLATE ENCODER/MULTIPLEXER DEVICES HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(3).	CAN TESTER FAULT ISOLATE BINARY ADDERS HARD WIRED TO UUT? (NO=1,YES=2)	0.200000E+01
(4).	CAN TESTER FAULT ISOLATE PARITY GENERATOR/CHECKER HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01
(5).	CAN TESTER FAULT ISOLATE DIGITAL COMPARATORS HARD WIRED TO UUT? (NO=1,YES=2)	0.100000E+01

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC)

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(1).	POLARITIES/VOLTAGE(S) MINIMUM	0.0	0.0	-.150000E+02
(2).	POLARITIES/VOLTAGE(S) MAXIMUM	0.500000E+01	0.150000E+02	0.0
(3).	ACCURACY	0.300000E+01	0.300000E+01	0.300000E+01
(4).	MAXIMUM CURRENT DRAIN	0.100000E+01	0.100000E+01	0.100000E+01
(5).	RIPPLE PEAK TO PEAK	0.0	0.0	0.0
(6).	ARE THEY FIXED OR PROGRAMMABLE? (F=1,P=2)	0.100000E+01	0.100000E+01	0.100000E+01
(7).	IF PROGRAMMABLE, IS IT CONTINUOUS OR INCREMENTAL? (C=1,I=2)	0.0	0.0	0.0

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T67 (POWER SUPPLY AND EXCITATION VOLTAGES - DC) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2	SET # 3
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.0	0.0
(9).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0	0.0
(10).	IF PROGRAMMABLE, IS IT BUS OR RESISTOR ORIENTED? (B=1,R=2)	0.0	0.0	0.0

PARAMETER GROUP: T68 (CLOCK RATES)

	DESCRIPTION	SET # 1	SET # 2
(1).	CLOCK RATE MINIMUM	0.0	0.140000E+04
(2).	CLOCK RATE MAXIMUM	0.400000E+08	0.180000E+07
(3).	CLOCK PULSE WIDTH MINIMUM	0.0	0.0
(4).	CLOCK PULSE WIDTH MAXIMUM	0.0	0.0
(5).	CLOCK RISE TIME MINIMUM	0.0	0.0
(6).	CLOCK RISE TIME MAXIMUM	0.0	0.0
(7).	CLOCK FALL TIME MINIMUM	0.0	0.0
(8).	CLOCK FALL TIME MAXIMUM	0.0	0.0
(9).	CLOCK RESOLUTION	0.0	0.0
(10).	CAN THE CLOCK RATES BE PROVIDED SIMULTANEOUSLY? (NO=1,YES=2)	0.200000E+01	0.200000E+01
(11).	HOW MANY CLOCK RATES ARE AVAILABLE PER TEST?	0.216000E+03	0.216000E+03
(12).	ARE THESE CLOCK RATES FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01	0.200000E+01

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(TABULATION BY TESTER)

PARAMETER GROUP: T68 (CLOCK RATES) - CONTINUED -

	DESCRIPTION	SET # 1	SET # 2
(13).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0	0.0
(14).	INCREMENTAL RANGE MAXIMUM?	0.0	0.0

PAPAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS)

NOTE: THIS GROUP WILL BE MATCHED TO P72 AND P74 IN THE DIGITAL PCB QUESTIONNAIRE

	DESCRIPTION	SET # 1
(1).	TIME INTERVAL MINIMUM	0.600000E-06
(2).	TIME INTERVAL MAXIMUM	0.160000E+02
(3).	RISE TIME MINIMUM	0.0
(4).	RISE TIME MAXIMUM	0.0
(5).	FALL TIME MINIMUM	0.0
(6).	FALL TIME MAXIMUM	0.0
(7).	PULSE WIDTH RANGE MINIMUM	0.250000E-07
(8).	PULSE WIDTH RANGE MAXIMUM	0.0
(9).	VOLTAGE RANGE MINIMUM	-.300000E+02
(10).	VOLTAGE RANGE MAXIMUM	0.300000E+02
(11).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01



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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T69 (GENERAL INPUT CHARACTERISTICS) - CONTINUED -

	DESCRIPTION	SET # 1
(12).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.600000E-06
(13).	INCREMENTAL RANGE MAXIMUM?	0.160000E+02

PARAMETER GROUP: T70 (LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.300000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.0
(3).	LOGIC LEVEL "0" MAXIMUM	0.0
(4).	LOGIC LEVEL "0" MINIMUM	-.300000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.216000E+03
(7).	ARE THESE LOGIC LEVELS FIXED OR PROGRAMMABLE? (F=1,P=2) ..	0.200000E+01
(8).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.150000E-01
(9).	INCREMENTAL RANGE MAXIMUM?	0.300000E+02

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* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T71 (SERIAL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.0
(2).	DATA BIT RATE MAXIMUM	0.180000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.0
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.216000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T72 GROUP. THE DIGITAL PCB GROUP P72 WILL BE MATCHED TO T69.

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(TABULATION BY TESTER)

PARAMETER GROUP: T73 (PARALLEL INPUT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.0
(2).	WORD RATE MAXIMUM	0.160000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.0
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.216000E+03
(9).	ARE THESE PARAMETERS FIXED OR PROGRAMMABLE? (F=1,P=2)	0.200000E+01
(10).	IF IT IS PROGRAMMABLE IN INCREMENTS, WHAT IS ITS INCREMENTAL RANGE MINIMUM?	0.0
(11).	INCREMENTAL RANGE MAXIMUM?	0.0

NOTE: THERE IS NO T74 GROUP. THE DIGITAL PCB GROUP P74 WILL BE MATCHED TO T69.

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(TABULATION BY TESTER)

PARAMETER GROUP: T75 (GENERAL OUTPUT MEASUREMENT CHARACTERISTICS)

DESCRIPTION	SET # 1
NOTE: THIS GROUP WILL BE MATCHED TO P78 AND P80 IN THE DIGITAL PCB QUESTIONNAIRE.	
(1). TIME INTERVAL MINIMUM	0.600000E-06
(2). TIME INTERVAL MAXIMUM	0.160000E+02
(3). RISE TIME MINIMUM	0.0
(4). RISE TIME MAXIMUM	0.0
(5). FALL TIME MINIMUM	0.0
(6). FALL TIME MAXIMUM	0.0
(7). PULSE WIDTH RANGE MINIMUM	0.0
(8). PULSE WIDTH RANGE MAXIMUM	0.0
(9). VOLTAGE RANGE MINIMUM	-.300000E+02
(10). VOLTAGE RANGE MAXIMUM	0.300000E+02
(11). IMPEDENCE	0.300000E+02
(12). IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(13). HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

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(TABULATION BY TESTER)

PARAMETER GROUP: T76 (OUTPUT LOGIC LEVELS)

	DESCRIPTION	SET # 1
(1).	LOGIC LEVEL "1" MAXIMUM	0.300000E+02
(2).	LOGIC LEVEL "1" MINIMUM	0.0
(3).	LOGIC LEVEL "0" MAXIMUM	0.0
(4).	LOGIC LEVEL "0" MINIMUM	-.300000E+02
(5).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.200000E+01
(6).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.216000E+03

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	DATA BIT RATE MINIMUM	0.0
(2).	DATA BIT RATE MAXIMUM	0.160000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.216000E+03
(5).	SEQUENCE LENGTH MINIMUM	0.0
(6).	SEQUENCE LENGTH MAXIMUM	0.0
(7).	IS THIS SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.216000E+03

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T77 (SERIAL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION	SET # 1

NOTE: THERE IS NO T78 GROUP. THE DIGITAL PCB GROUP P78 WILL BE MATCHED TO T75.

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS)

	DESCRIPTION	SET # 1
(1).	WORD RATE MINIMUM	0.0
(2).	WORD RATE MAXIMUM	0.160000E+07
(3).	WORD LENGTH MINIMUM	0.0
(4).	WORD LENGTH MAXIMUM	0.216000E+03
(5).	WORD SEQUENCE LENGTH MINIMUM	0.0
(6).	WORD SEQUENCE LENGTH MAXIMUM	0.216000E+03
(7).	IS THIS A SIMULTANEOUS CAPABILITY? (NO=1,YES=2)	0.0
(8).	HOW MANY OF THIS SET ARE AVAILABLE SIMULTANEOUSLY?	0.0

NOTE: THERE IS NO T80 GROUP. THE DIGITAL PCB

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * DIGITAL PCB TESTER CAPABILITY SUMMARY * * *

(TABULATION BY TESTER)

PARAMETER GROUP: T79 (PARALLEL OUTPUT MEASUREMENT CHARACTERISTICS) - CONTINUED -

DESCRIPTION SET # 1

GROUP P80 WILL BE MATCHED TO T75.

SECTION IIC
D/PCB TEST SYSTEM SPECIFICATION

Digital Printed Circuit Board

Test System

Specification

Date: 21 May 1979

Prepared by: A. F. Lee

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1.0 SCOPE - This specification defines functional performance requirements for a Digital Printed Circuit Board Test System. The Digital Printed Circuit Board Test System will hereafter be referred to as the System.

2.0 APPLICABLE DOCUMENTS - To be determined.

3.0 REQUIREMENTS

3.1 System Definition - The System shall have equipment that is designed to provide stimulus and measurement testing capabilities for a digital printed circuit board (D/PCB) in a production test environment. The System shall test, analyze, evaluate and fault isolate the functional parameters of a digital printed circuit board, and other electronics required to fulfill the requirements of this specification.

3.2 Characteristics

3.2.1 Performance - The System shall meet, or exceed the performance requirements specified herein.

3.2.1.1 System Performance Characteristics

3.2.1.1.1 Logic Families - The System shall have the capability to test two or more mixed logic families on a Unit Under Test (UUT). The logic families will be determined by the logic "Low" Range and the Logic "High" Range for the drivers and the Threshold Range for the receivers as specified in paragraphs 3.2.1.2.2.2 and 3.2.1.2.2.3, respectively.

3.2.1.1.2 Fault Isolation - The System shall have the capability to fault isolate a Digital PCB to a component or an IC with up to 40 pins.

3.2.1.1.3 Input/Output Pins - The System shall have capability to test a digital printed circuit board with 256 Input/Output pins.

3.2.1.1.4 Circuit Complexity - The System shall have the capability to functionally test a digital circuit board with a circuit complexity greater than 25,000 equivalent gates.

3.2.1.1.4.1 Test Comprehensiveness - The System shall provide the ability to grade the test comprehensiveness of a test program (in terms of proportion of faults detected).

3.2.1.1.5 Test Pattern Frequency - The System shall have the capability to provide a test rate of not less than 10,000 patterns per second for a single pin.

3.2.1.1.6 Prime Power

3.2.1.1.6.1 AC Power

The System shall be designed to operate from alternating current power having characteristics as specified herein:

115 volts ± 5%, alternating current (Vac)
50 or 60 Hertz (Hz), single phase

3.2.1.2 Functional Subsystems - The System shall consist of five subsystems as shown in Figure I and shall meet the requirements specified in the following sub-paragraphs.

3.2.1.2.1 Mini Computer and Peripherals Subsystem

3.2.1.2.1.1 Mini Computer - The Mini Computer shall have not less than 12 I/O channels and a memory capacity of not less than 32K bytes.

3.2.1.2.1.2 Disc Controller - The Disc Controller shall interface with a single computer I/O channel. It receives commands from the computer and controls data transfers between the computer and the disc units according to the computer command.

3.2.1.2.1.2.1 Disc Unit(s) - The System shall provide two disc drives. The disc unit(s) shall interface with the disc controller and each disc unit shall provide a memory storage capacity of not less than 2.5 Megabytes.

3.2.1.2.1.3 Mass Storage - The System shall provide at least 256K bytes of data storage in a form that is compatible to the System, such as a floppy disc, cartridge, cassette, etc.

3.2.1.2.1.4 Line Printer - The System shall provide a line printer that can print out program listings and reports in 132 columns and print at a minimum rate of 200 Lines Per Minute (LPM).

3.2.1.2.2 Digital Test System

3.2.1.2.2.1 Programmable Logic Drivers/Receivers - The System shall provide 256 programmable logic drivers/receivers. Each logic family to be tested on a UUT shall be independently programmed over a ±15 volt range.

3.2.1.2.2.2 Drivers - The System shall provide drivers with the following specification:

Logic "Low" Range:	-15v to +15v
Logic "High" Range:	-15v to +15 v
Static Accuracy:	±0.15v
Voltage Resolution:	8 mv
Slew Rate:	40 volts/usec
Current Source:	16 mA to 12 volts
Current Sink:	16 mA to 12 volts

3.2.1.2.2.3 Receivers - The System shall provide receivers with the following specification:

Threshold Range:	-15v to +15v
Static Accuracy:	±0.15v
Voltage Resolution:	8mV

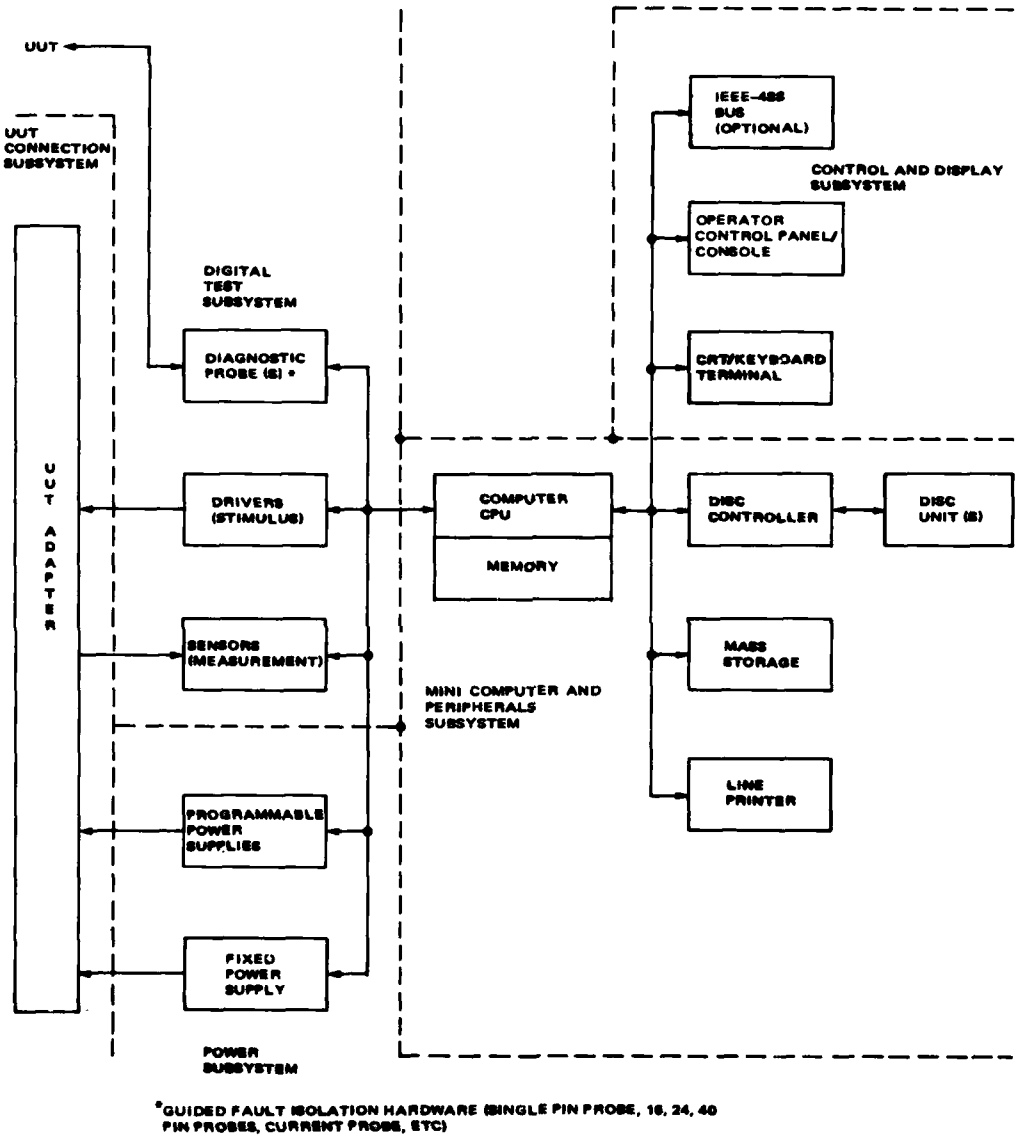


Figure I. Test System Block Diagram.

3.2.1.2.2.4 Digital Clock - The System shall provide digital clocks with the following specification:

"Low" Range:	-15v to +15v
"High" Range:	-15v to +15v
Voltage Resolution:	8mV
Frequency:	up to 2 MHz
Frequency Accuracy:	±0.1%

3.2.1.2.2.5 Diagnostic Probes - The System shall have diagnostic probe and/or clips to aid the operator in troubleshooting a UUT and isolating a fault to a defective DPCB component or IC. The diagnostic probe shall have up to 40 pin capacity. The System shall provide a current sensor to enhance the System's fault isolation capability.

3.2.1.2.3 Control and Display Subsystem

3.2.1.2.3.1 Operator Terminal (CRT/Keyboard) - The System shall provide a CRT Terminal with keyboard and internal memory for display of up to 24 lines of text at 80 characters per line.

3.2.1.2.3.2 Control Panel/Console - The System shall provide a Control Panel/Console that is designed to contain all the controls and indicators necessary for testing and troubleshooting the UUT. The Control Panel/Console shall also provide the use of a footswitch for hands-free operation during testing.

3.2.1.2.3.3 IEEE-488-1975 Bus (optional) - The System shall provide a IEEE 488 Bus Interface.

3.2.1.2.4.1 Programmable Power Supplies - The System shall provide 3 programmable power supplies with the following specifications:

	1.	2.	3.	Unit
Voltage Range:	±0-10	±0-20	±0-40	volts
Voltage Resolution:	5	10	20	millivolts
Voltage Accuracy:	±0.1%	±0.1%	±0.1%	of FS Range
Current Range:	12	3	2	Amperes
Current Limit Resolution:	±0.3%	±0.3%	±0.3%	Full Scale
Current Limit Accuracy:	±1%	±1%	±1%	of FS Range

3.2.1.2.4.2 Fixed Power Supply - The System shall provide 1 fixed power supply with the following specifications:

Voltage:	4v to 7v (set @ 5v)
Current:	10 Amps max
Voltage Accuracy:	±1%
Load Regulation:	±10mV

3.2.1.2.5 UUT Connection Subsystem

3.2.1.2.5.1 Test Fixture - The System shall provide the test fixture required to interface with the Unit Under Test (UUT) adapter.

3.2.1.3 Software - The System shall include the following software packages to meet, or exceed the performance requirements of this specification.

a. Operational Software
b. System's Digital Simulator
c. System's Self-Test
d. Data Base Management System
e. Components Library

3.2.1.4 Environmental Conditions

3.2.1.4.1 Temperature - The System shall withstand the effects of ambient air temperature as follows:

a. Operating Temperature - The System shall operate without degraded performance at any temperature between +10 degree centigrade and +40 degree centigrade.

b. Non-operating Temperature - The System after exposure to non-operating temperature of -40 degree centigrade and +65 degree centigrade shall operate without degraded performance when restored to the normal operating temperature range.

3.2.1.4.2 Humidity - The System shall maintain specified performance when exposed to relative humidity of up to 80 percent for continuous and intermittent periods.

3.2.1.5 Manuals - The following manuals shall be provided with the System:

a. Operating
b. Programming
c. Servicing

3.2.1.6 Training - The manufacturer shall provide the following training courses for two people:

a. Tester Operating and Programming
b. Tester Maintenance

3.2.1.7 Installation and Acceptance Test - The System shall be installed by tester manufacturer personnel and an acceptance test shall be performed. Acceptance test criteria must be approved by Hughes Aircraft Company, Fullerton, prior to test date.

3.2.1.8 Transportability - The System shall be capable of transport by highway, rail, water, or air.

INTERIM REPORT ATT III – MM&T – DFI FOR PCBs – PERFORMANCE EVALUATION

PERFORMANCE EVALUATION –

ATTACHMENT III – TO INTERIM REPORT (BASIC EFFORT)

MANUFACTURING METHODS AND TECHNOLOGY FOR 'DIGITAL FAULT ISOLATION FOR PRINTED CIRCUIT BOARDS'

PROJECT NO. R783242

CONTRACT DAAK40-78-C-0290
25 AUGUST 1979
CDRL A003

CLASSIFICATION

FR 79-12-005
99231

170 - GS 3/66

PERFORMANCE EVALUATION

ATTACHMENT III

TO INTERIM REPORT (BASIC EFFORT)

Manufacturing Methods and Technology for

'Digital Fault Isolation for Printed Circuit Boards'

Project No. R783242

Prepared for

U.S. Army Missile Research and Development Command

Redstone Arsenal, Alabama 35809

Project Officer: G. Little
DRDMI-EAT
(205)-876-3848

Contract No. DAAK 40-78-C-0290
CDRL A003

Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

Report Date: 25 August 1979
FR79-12-669

12-484

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Rev. Jan. 1971 Vendor's Name

FOREWORD

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards containing complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the development of digital fault isolation methodology, and the identification of the corresponding optimum available automatic test hardware.

The subsequent contract option phase of this project involves the purchase, setup, and demonstration of the selected fault isolation hardware/software system, using the developed techniques.

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SECTION III B – MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS

SECTION III C – TESTER EVALUATION FACTORS

SECTION III D – COST PERFORMANCE EVALUATION

SECTION III E – TESTER COMPOSITE SCORES

SECTION III F – TEST SYSTEM MEASURED PERFORMANCE

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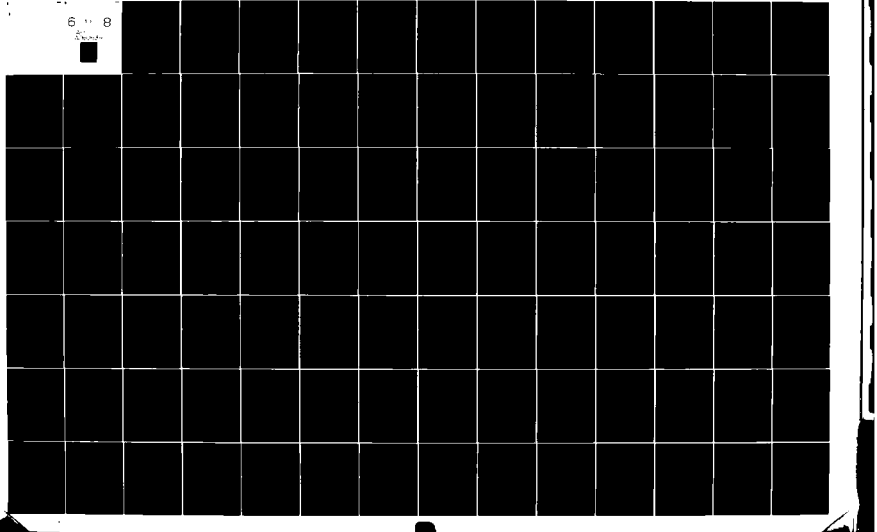
SECTION IIIA
MATCHUP ALGORITHMS

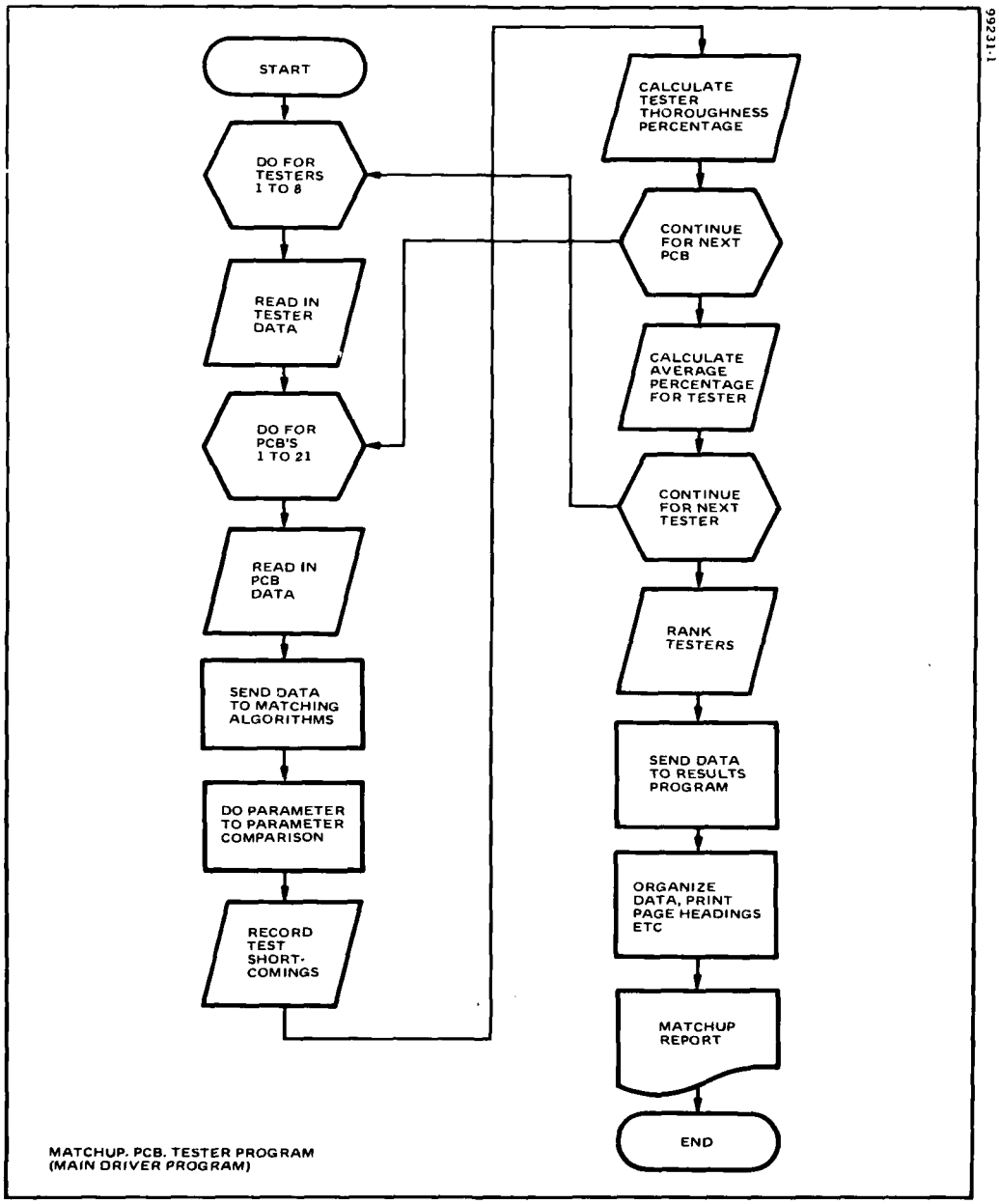
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MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
AUG 79 DAAK40-78-C-0290
UNCLASSIFIED HAC-FR79-18-669A NL

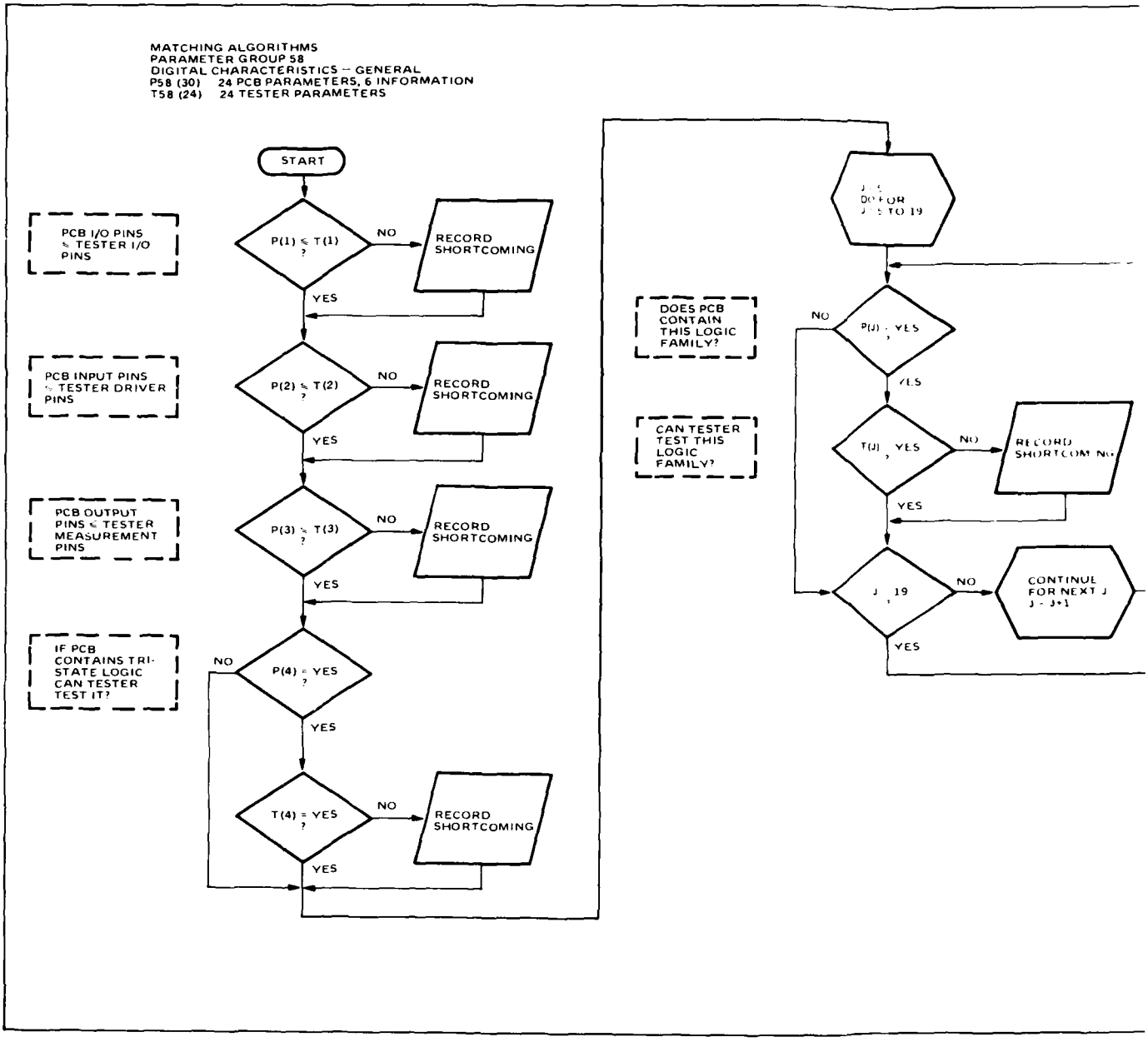




MATCHUP. PCB. TESTER PROGRAM
(MAIN DRIVER PROGRAM)

IIIA-0

MATCHING ALGORITHMS
PARAMETER GROUP 58
DIGITAL CHARACTERISTICS – GENERAL
P58 (30) 24 PCB PARAMETERS, 6 INFORMATION
T58 (24) 24 TESTER PARAMETERS

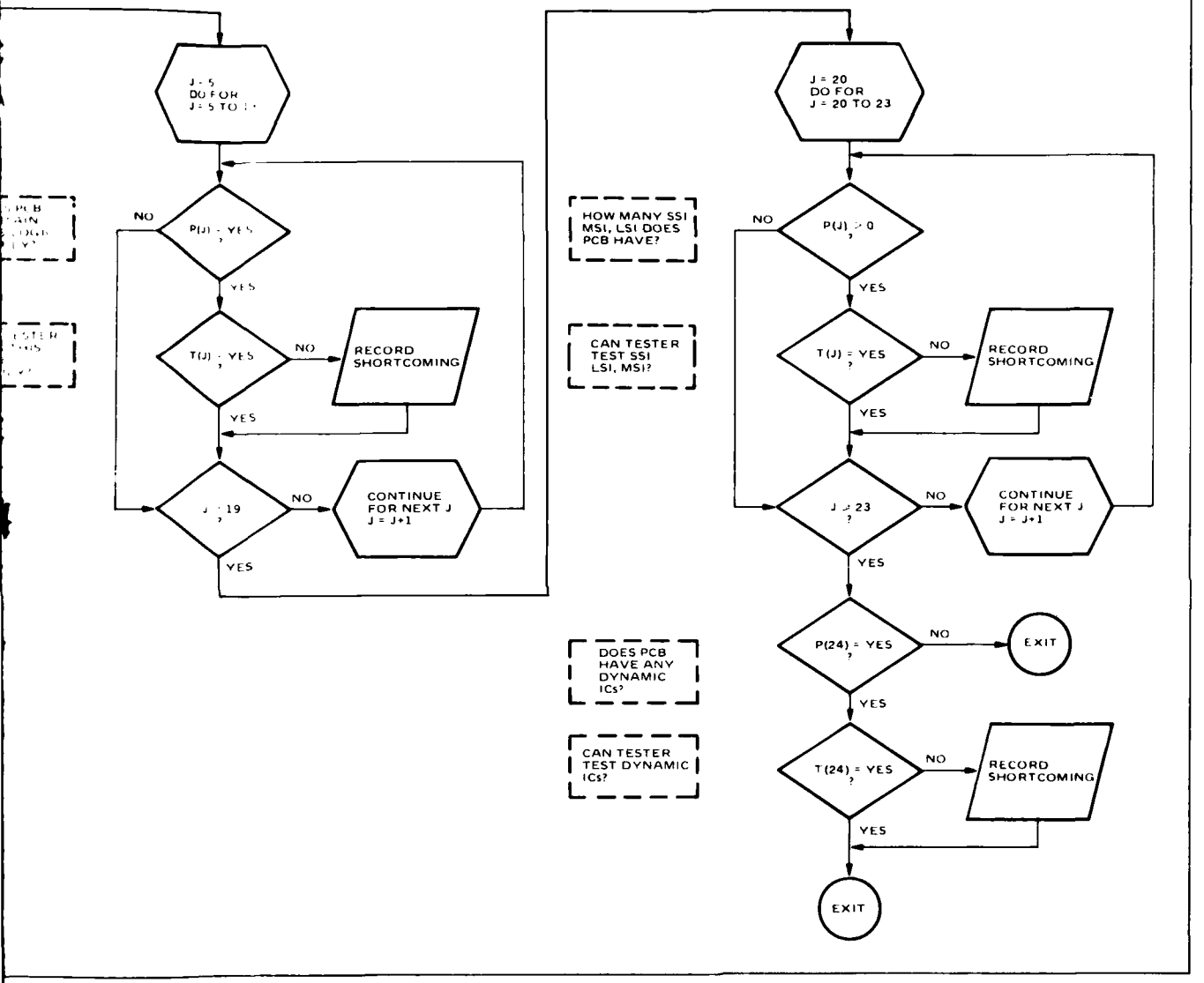


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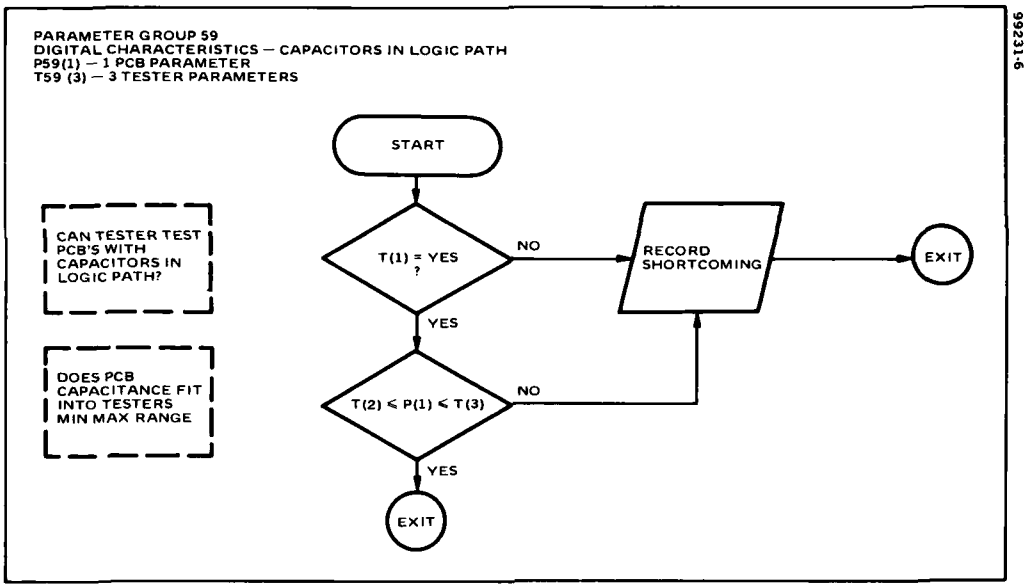
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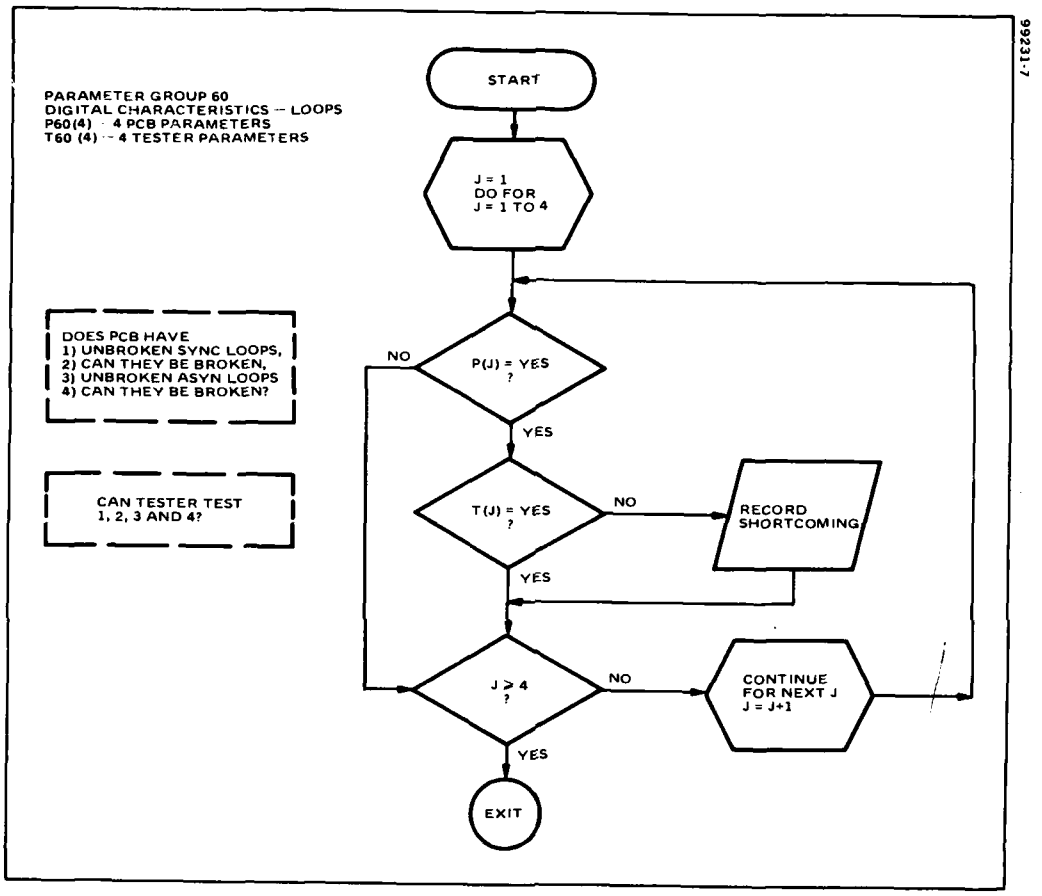
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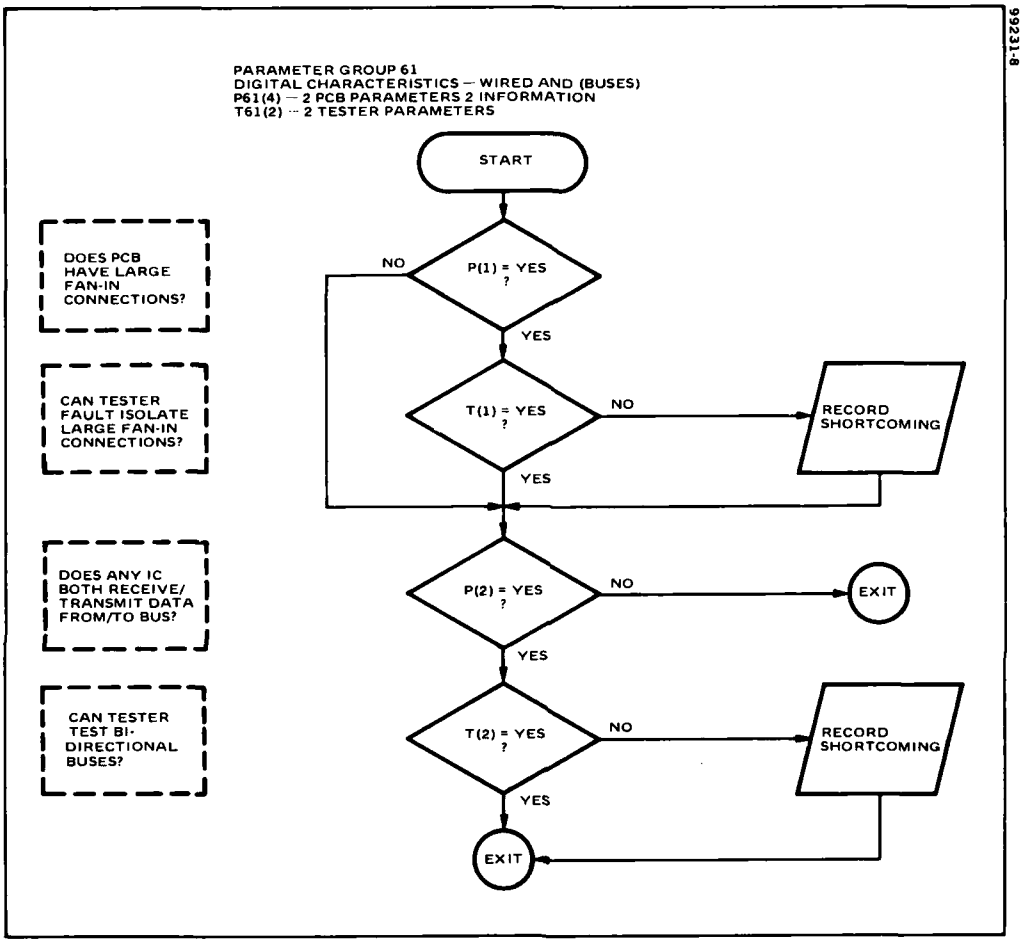
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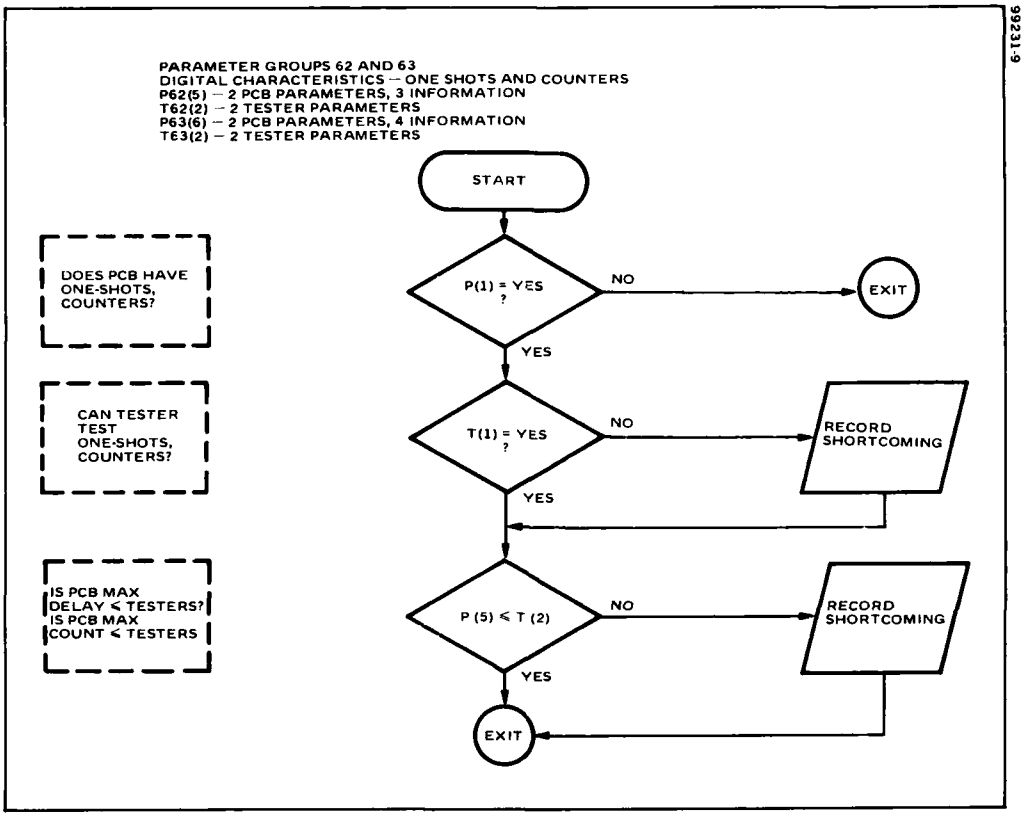
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PARAMETER GROUP 59
DIGITAL CHARACTERISTICS — CAPACITORS IN LOGIC PATH
P59(1) — 1 PCB PARAMETER
T59 (3) — 3 TESTER PARAMETERS

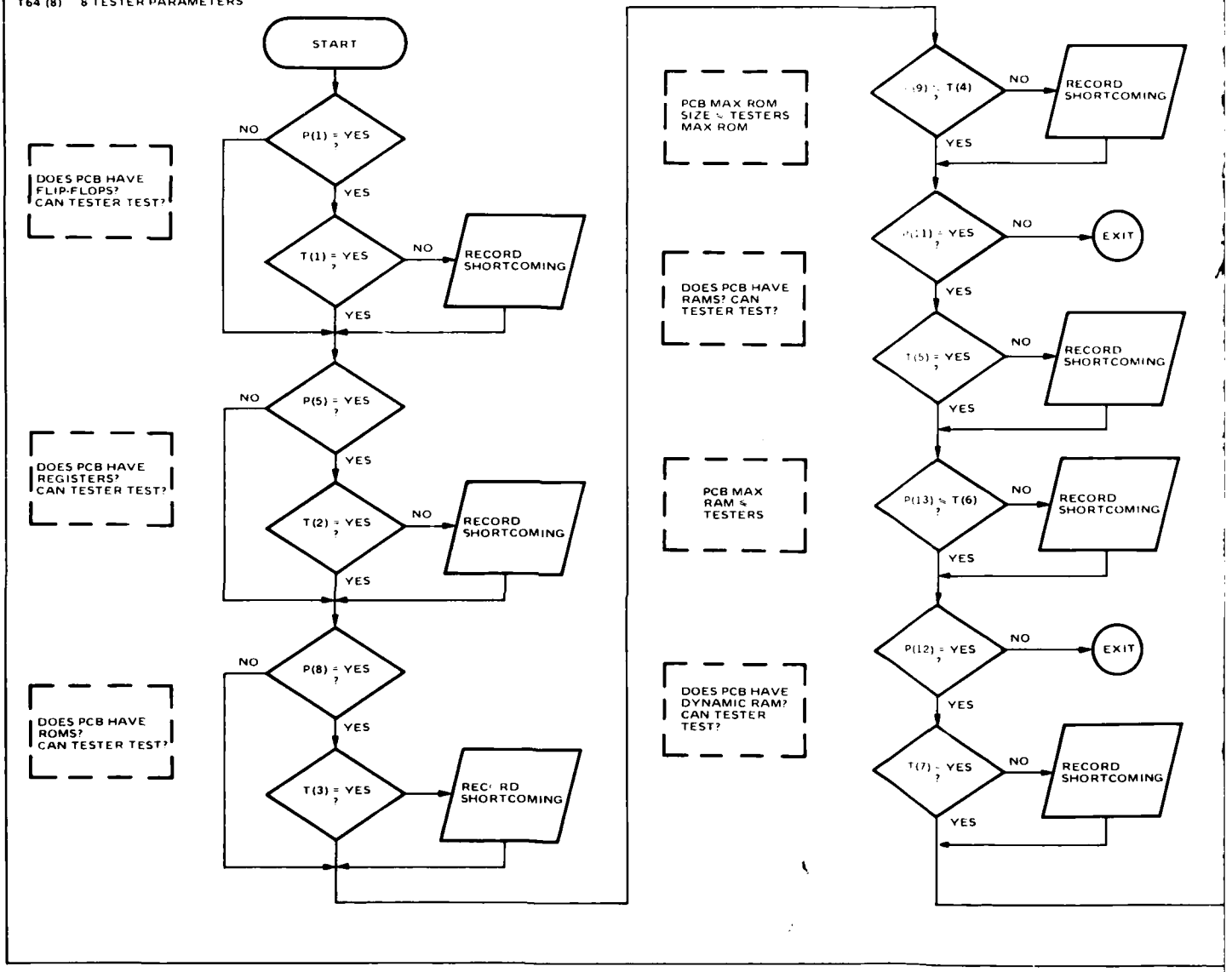



PARAMETER GROUP 60
DIGITAL CHARACTERISTICS -- LOOPS
P60(4) -- 4 PCB PARAMETERS
T60 (4) -- 4 TESTER PARAMETERS
DOES PCB HAVE
1) UNBROKEN SYNC LOOPS,
2) CAN THEY BE BROKEN,
3) UNBROKEN ASYN LOOPS
4) CAN THEY BE BROKEN?
CAN TESTER TEST
1, 2, 3 AND 4?
START
J = 1
DO FOR
J = 1 TO 4
P(J) = YES
?
NO
YES
T(J) = YES
?
NO
RECORD
SHORTCOMING
YES
J ≥ 4
?
NO
CONTINUE
FOR NEXT J
J = J+1
YES
EXIT
99231-7


99231-8
PARAMETER GROUP 61
DIGITAL CHARACTERISTICS — WIRED AND (BUSES)
P61(4) — 2 PCB PARAMETERS 2 INFORMATION
T61(2) — 2 TESTER PARAMETERS
START
DOES PCB HAVE LARGE FAN-IN CONNECTIONS?
P(1) = YES ?
NO
YES
CAN TESTER FAULT ISOLATE LARGE FAN-IN CONNECTIONS?
T(1) = YES ?
NO
RECORD SHORTCOMING
YES
DOES ANY IC BOTH RECEIVE/ TRANSMIT DATA FROM/TO BUS?
P(2) = YES ?
NO
EXIT
YES
CAN TESTER TEST BI-DIRECTIONAL BUSES?
T(2) = YES ?
NO
RECORD SHORTCOMING
YES
EXIT


PARAMETER GROUPS 62 AND 63
DIGITAL CHARACTERISTICS – ONE SHOTS AND COUNTERS
P62(5) – 2 PCB PARAMETERS, 3 INFORMATION
T62(2) – 2 TESTER PARAMETERS
P63(6) – 2 PCB PARAMETERS, 4 INFORMATION
T63(2) – 2 TESTER PARAMETERS
START
DOES PCB HAVE ONE-SHOTS, COUNTERS?
P(1) = YES ?
NO
EXIT
YES
CAN TESTER TEST ONE-SHOTS, COUNTERS?
T(1) = YES ?
NO
RECORD SHORTCOMING
YES
IS PCB MAX DELAY ≤ TESTERS? IS PCB MAX COUNT ≤ TESTERS
P (5) ≤ T (2)
NO
RECORD SHORTCOMING
YES
EXIT
9923I-9

PARAMETER GROUP 64
DIGITAL CHARACTERISTICS STORAGE ELEMENTS
P64(17) = 8 PCB PARAMETERS, 9 INFORMATION
T64 (8) 8 TESTER PARAMETERS

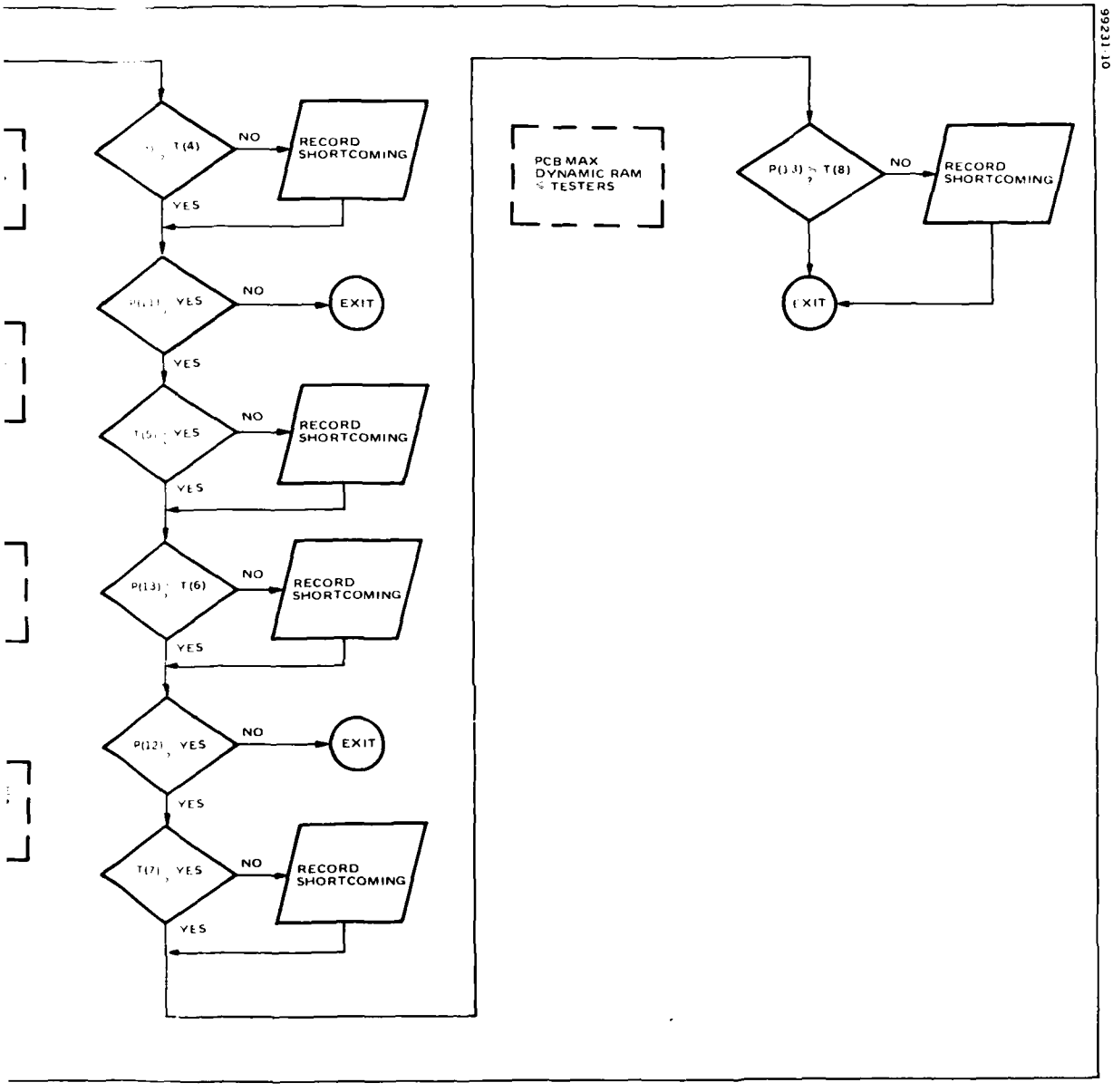


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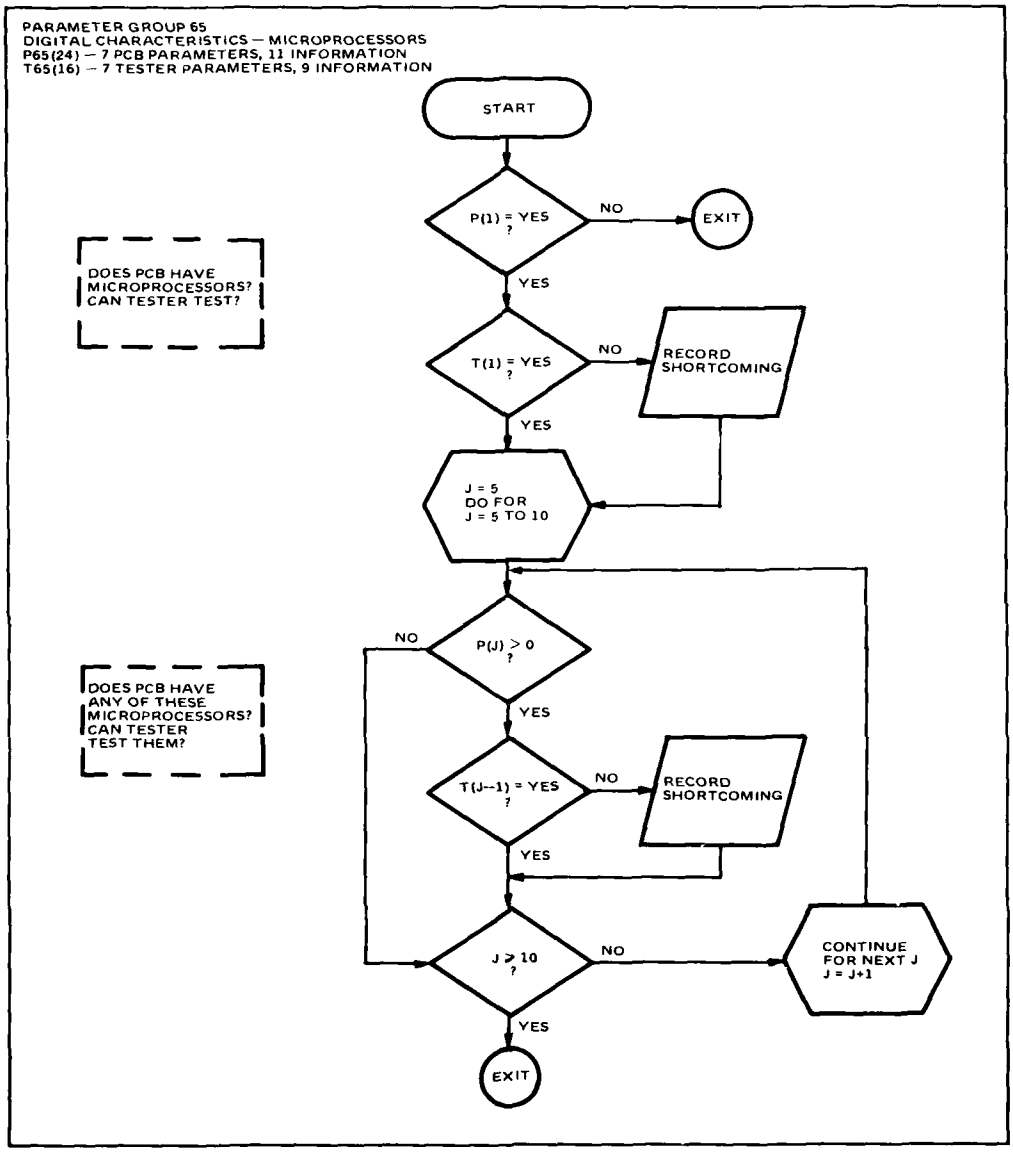


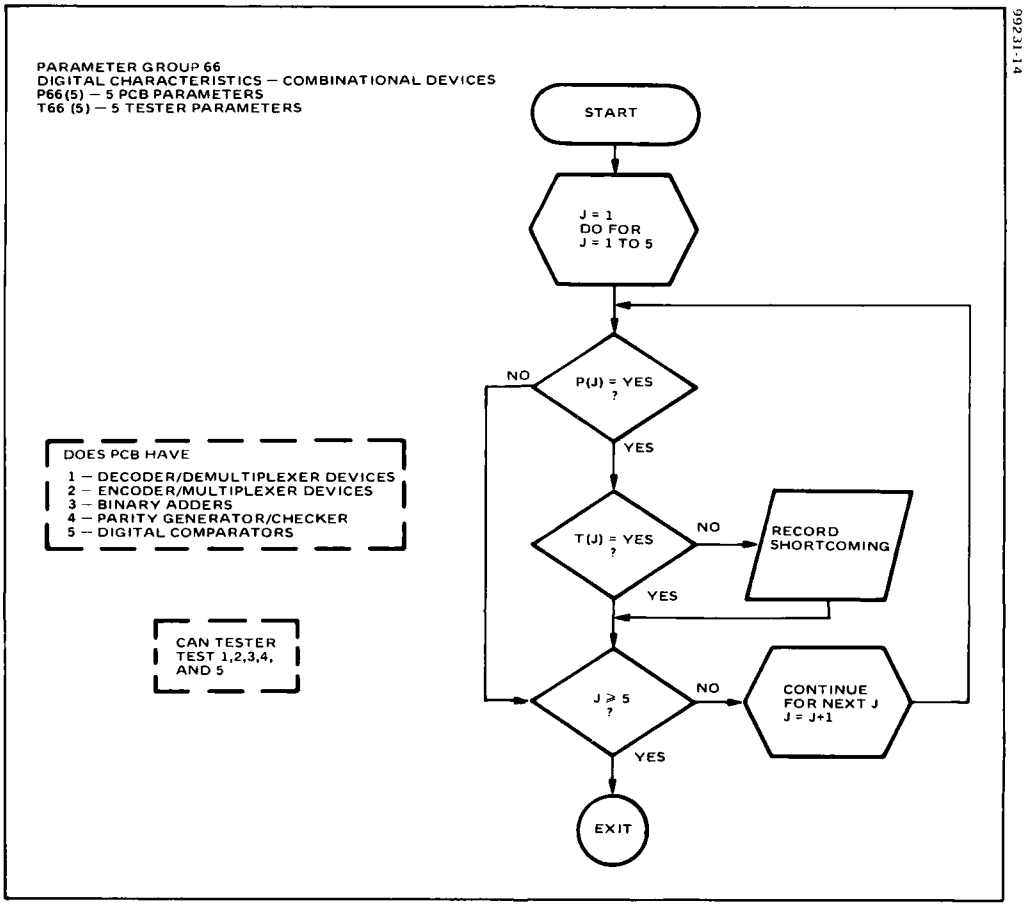
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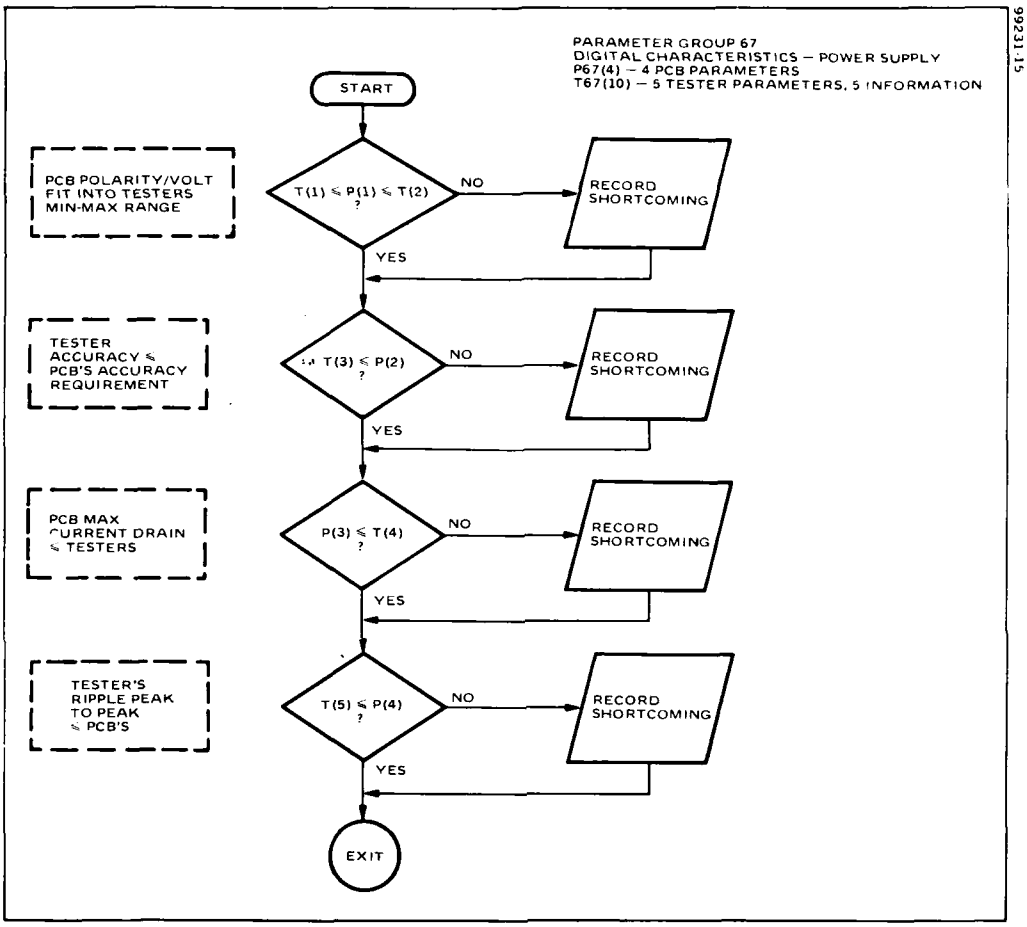
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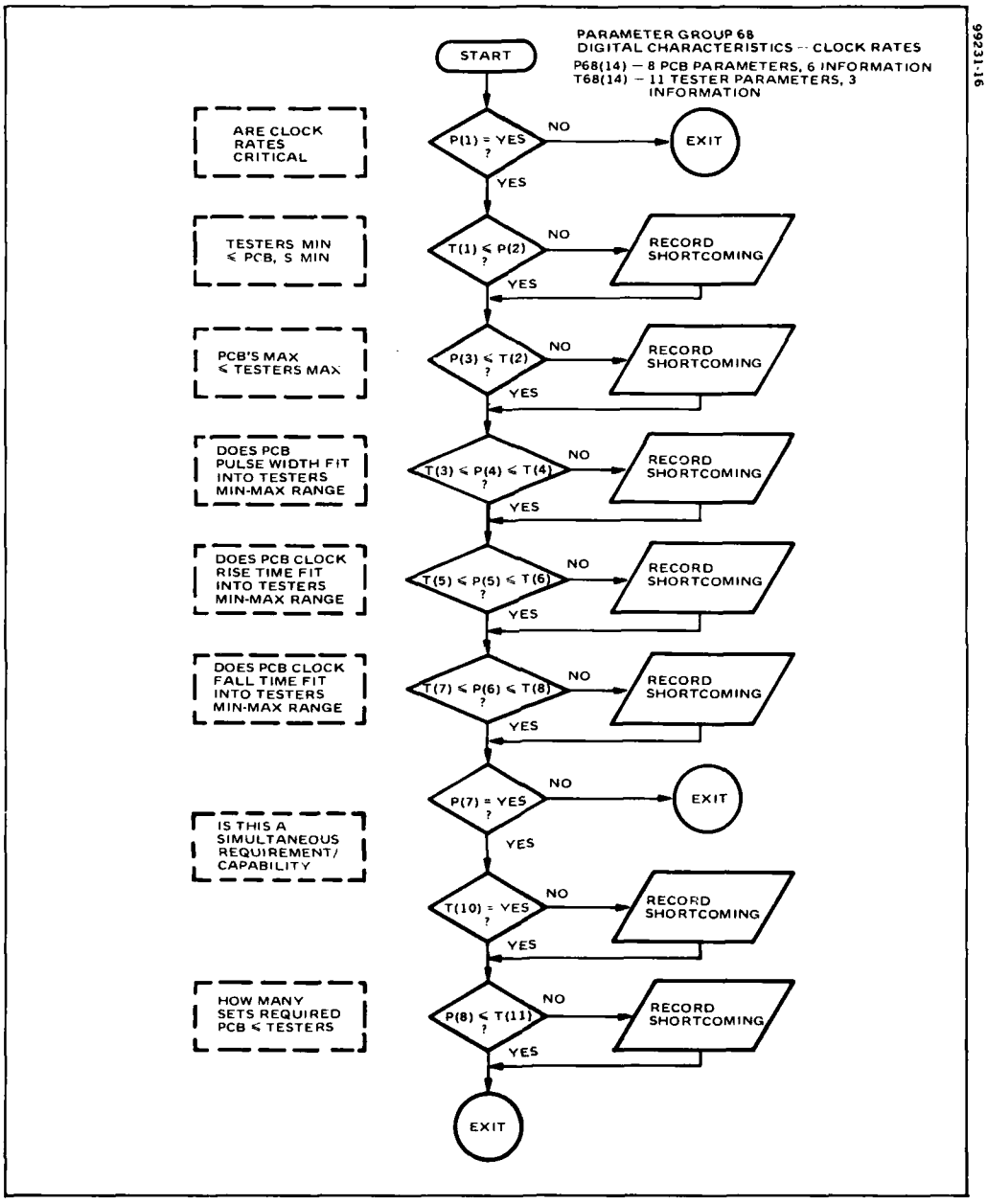
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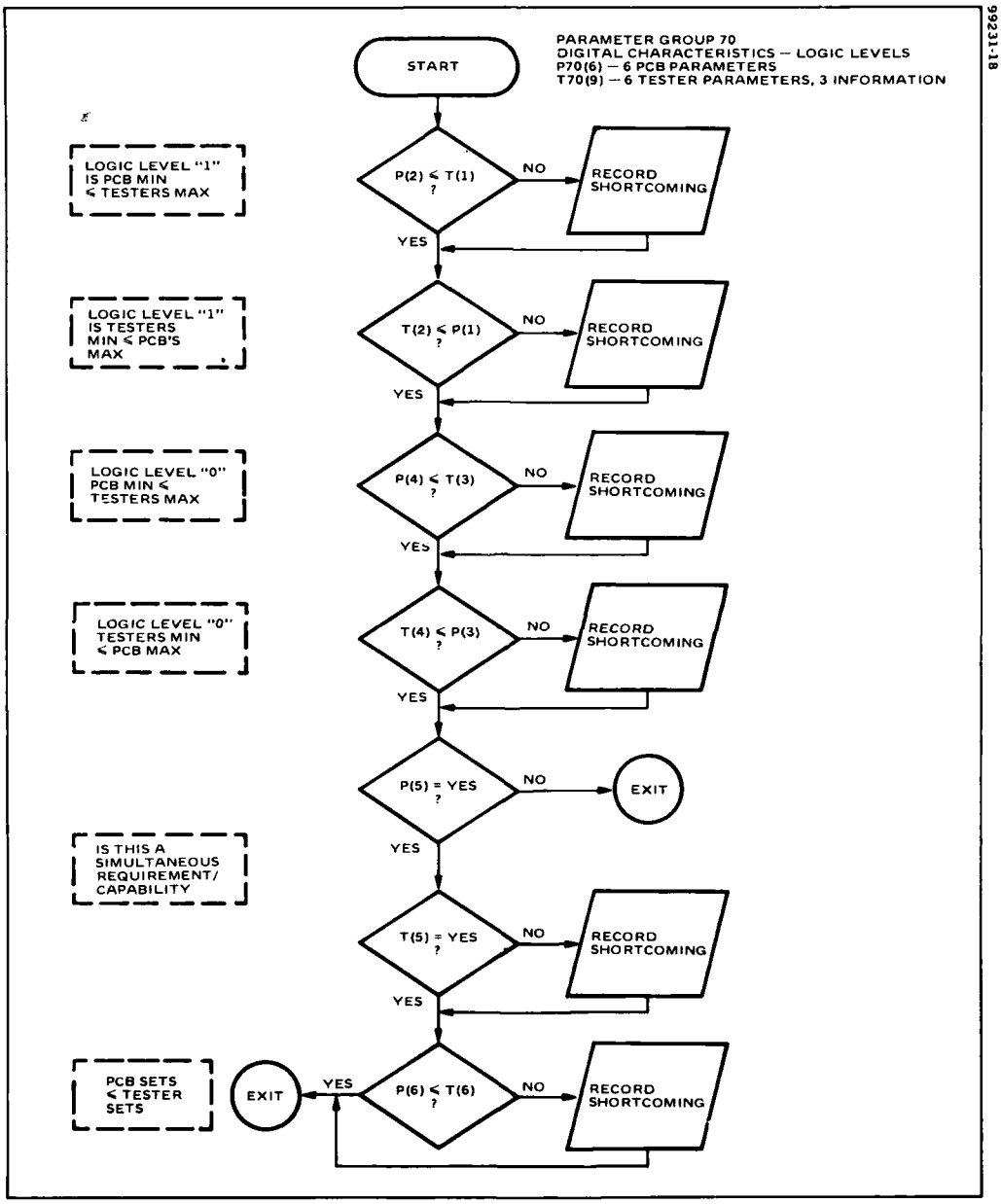
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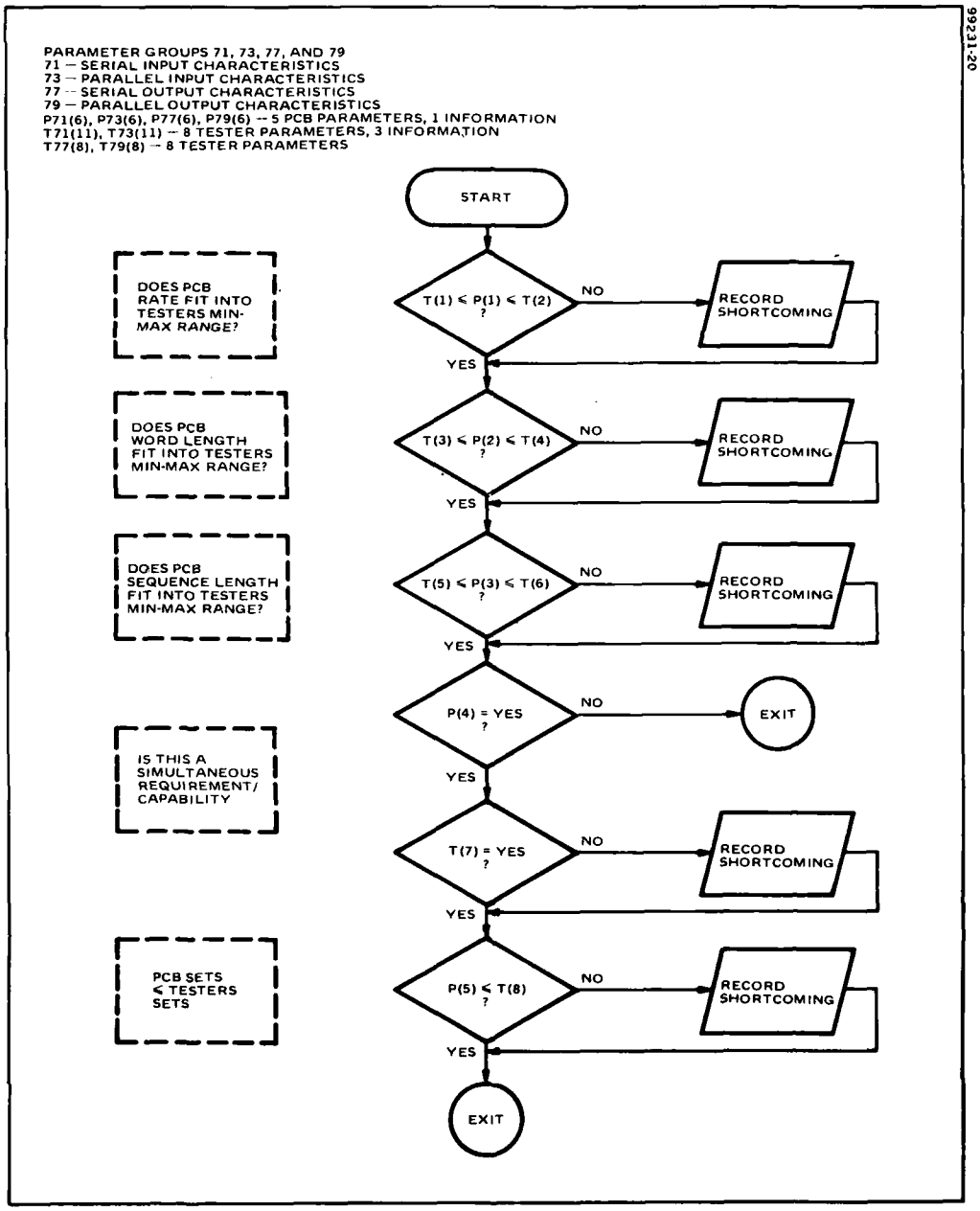

PARAMETER GROUP 65
DIGITAL CHARACTERISTICS — MICROPROCESSORS
P65(24) — 7 PCB PARAMETERS, 11 INFORMATION
T65(16) — 7 TESTER PARAMETERS, 9 INFORMATION
99231-13
START
P(1) = YES ?
NO
EXIT
YES
DOES PCB HAVE MICROPROCESSORS? CAN TESTER TEST?
T(1) = YES ?
NO
RECORD SHORTCOMING
YES
J = 5
DO FOR J = 5 TO 10
NO
P(J) > 0 ?
YES
DOES PCB HAVE ANY OF THESE MICROPROCESSORS? CAN TESTER TEST THEM?
T(J--1) = YES ?
NO
RECORD SHORTCOMING
YES
J > 10 ?
NO
CONTINUE FOR NEXT J
J = J+1
YES
EXIT


PARAMETER GROUP 66
DIGITAL CHARACTERISTICS – COMBINATIONAL DEVICES
P66(5) – 5 PCB PARAMETERS
T66 (5) – 5 TESTER PARAMETERS
DOES PCB HAVE
1 – DECODER/DEMULTIPLEXER DEVICES
2 – ENCODER/MULTIPLEXER DEVICES
3 – BINARY ADDERS
4 – PARITY GENERATOR/CHECKER
5 – DIGITAL COMPARATORS
CAN TESTER TEST 1,2,3,4, AND 5
START
J = 1
DO FOR
J = 1 TO 5
P(J) = YES ?
NO
YES
T(J) = YES ?
NO
RECORD SHORTCOMING
YES
J ≥ 5 ?
NO
CONTINUE FOR NEXT J
J = J+1
YES
EXIT
6923I-14


PARAMETER GROUP 67
DIGITAL CHARACTERISTICS – POWER SUPPLY
P67(4) – 4 PCB PARAMETERS
T67(10) – 5 TESTER PARAMETERS, 5 INFORMATION
99231-15
START
PCB POLARITY/VOLT FIT INTO TESTERS MIN-MAX RANGE
T(1) ≤ P(1) ≤ T(2) ?
NO
RECORD SHORTCOMING
YES
TESTER ACCURACY ≤ PCB'S ACCURACY REQUIREMENT
T(3) ≤ P(2) ?
NO
RECORD SHORTCOMING
YES
PCB MAX CURRENT DRAIN ≤ TESTERS
P(3) ≤ T(4) ?
NO
RECORD SHORTCOMING
YES
TESTER'S RIPPLE PEAK TO PEAK ≤ PCB'S
T(5) ≤ P(4) ?
NO
RECORD SHORTCOMING
YES
EXIT

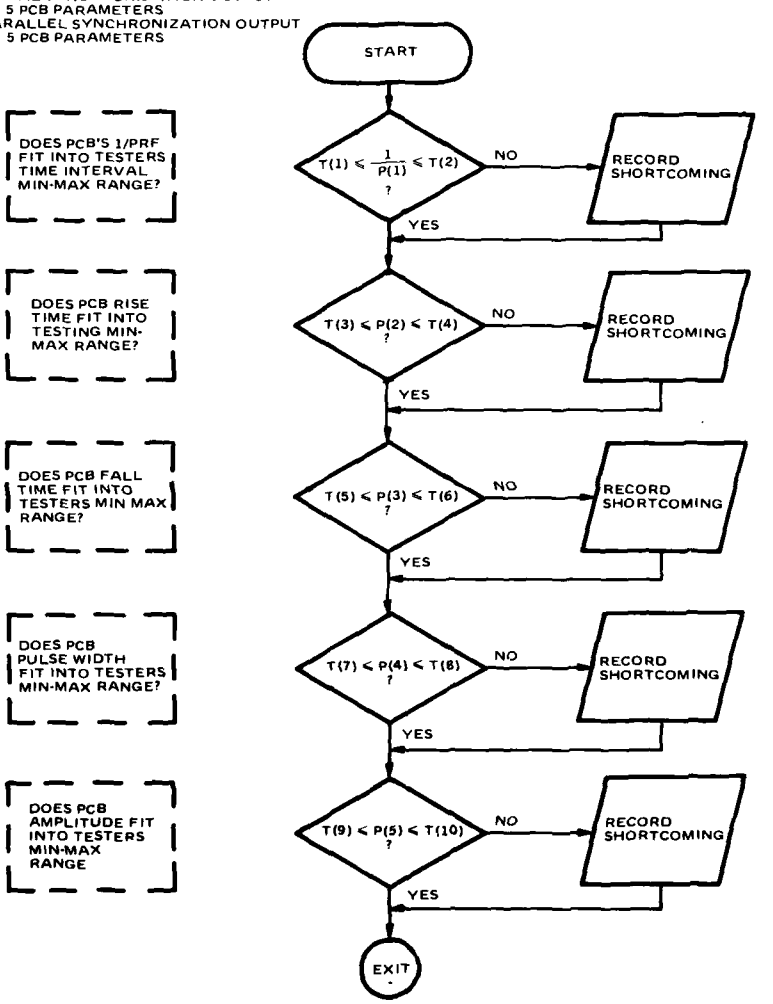

PARAMETER GROUP 68
DIGITAL CHARACTERISTICS -- CLOCK RATES
P68(14) – 8 PCB PARAMETERS, 6 INFORMATION
T68(14) – 11 TESTER PARAMETERS, 3 INFORMATION
START
ARE CLOCK RATES CRITICAL
P(1) = YES ?
NO
EXIT
YES
TESTERS MIN ≤ PCB, S MIN
T(1) ≤ P(2) ?
NO
RECORD SHORTCOMING
YES
PCB'S MAX ≤ TESTERS MAX
P(3) ≤ T(2) ?
NO
RECORD SHORTCOMING
YES
DOES PCB PULSE WIDTH FIT INTO TESTERS MIN-MAX RANGE
T(3) ≤ P(4) ≤ T(4) ?
NO
RECORD SHORTCOMING
YES
DOES PCB CLOCK RISE TIME FIT INTO TESTERS MIN-MAX RANGE
T(5) ≤ P(5) ≤ T(6) ?
NO
RECORD SHORTCOMING
YES
DOES PCB CLOCK FALL TIME FIT INTO TESTERS MIN-MAX RANGE
T(7) ≤ P(6) ≤ T(8) ?
NO
RECORD SHORTCOMING
YES
P(7) = YES ?
NO
EXIT
YES
IS THIS A SIMULTANEOUS REQUIREMENT/ CAPABILITY
T(10) = YES ?
NO
RECORD SHORTCOMING
YES
HOW MANY SETS REQUIRED PCB ≤ TESTERS
P(8) ≤ T(11) ?
NO
RECORD SHORTCOMING
YES
EXIT
99231-16


99231-18
PARAMETER GROUP 70
DIGITAL CHARACTERISTICS — LOGIC LEVELS
P70(6) — 6 PCB PARAMETERS
T70(9) — 6 TESTER PARAMETERS, 3 INFORMATION
START
LOGIC LEVEL "1" IS PCB MIN ≤ TESTERS MAX
P(2) ≤ T(1) ?
NO
RECORD SHORTCOMING
YES
LOGIC LEVEL "1" IS TESTERS MIN ≤ PCB'S MAX
T(2) ≤ P(1) ?
NO
RECORD SHORTCOMING
YES
LOGIC LEVEL "0" PCB MIN ≤ TESTERS MAX
P(4) ≤ T(3) ?
NO
RECORD SHORTCOMING
YES
LOGIC LEVEL "0" TESTERS MIN ≤ PCB MAX
T(4) ≤ P(3) ?
NO
RECORD SHORTCOMING
YES
P(5) = YES ?
NO
EXIT
YES
IS THIS A SIMULTANEOUS REQUIREMENT/ CAPABILITY
T(5) = YES ?
NO
RECORD SHORTCOMING
YES
PCB SETS ≤ TESTER SETS
EXIT
YES
P(6) ≤ T(6) ?
NO
RECORD SHORTCOMING

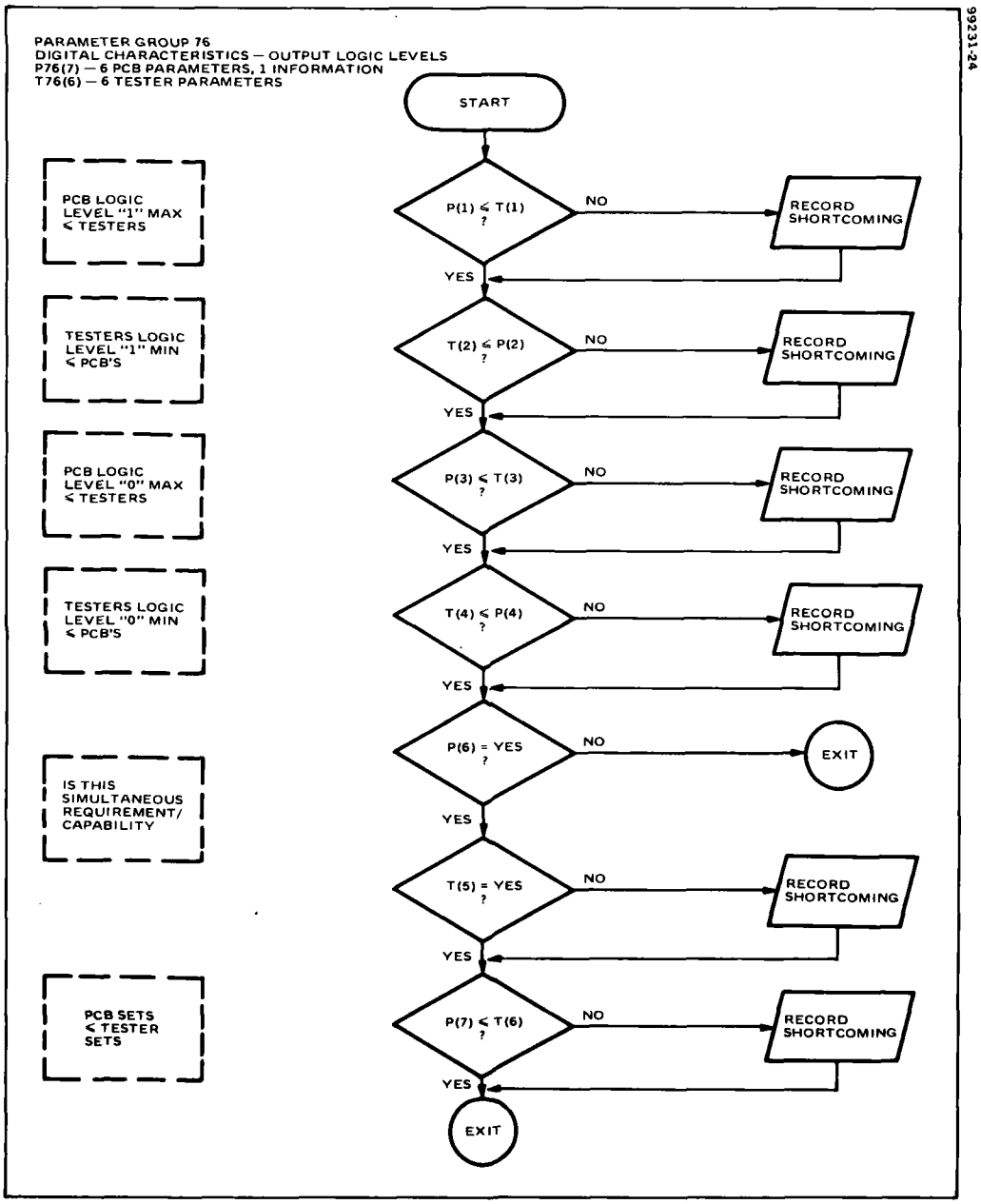

PARAMETER GROUPS 71, 73, 77, AND 79
71 — SERIAL INPUT CHARACTERISTICS
73 — PARALLEL INPUT CHARACTERISTICS
77 — SERIAL OUTPUT CHARACTERISTICS
79 — PARALLEL OUTPUT CHARACTERISTICS
P71(6), P73(6), P77(6), P79(6) — 5 PCB PARAMETERS, 1 INFORMATION
T71(11), T73(11) — 8 TESTER PARAMETERS, 3 INFORMATION
T77(8), T79(8) — 8 TESTER PARAMETERS
99231-20
START
DOES PCB RATE FIT INTO TESTERS MIN-MAX RANGE?
T(1) ≤ P(1) ≤ T(2) ?
NO
RECORD SHORTCOMING
YES
DOES PCB WORD LENGTH FIT INTO TESTERS MIN-MAX RANGE?
T(3) ≤ P(2) ≤ T(4) ?
NO
RECORD SHORTCOMING
YES
DOES PCB SEQUENCE LENGTH FIT INTO TESTERS MIN-MAX RANGE?
T(5) ≤ P(3) ≤ T(6) ?
NO
RECORD SHORTCOMING
YES
P(4) = YES ?
NO
EXIT
YES
IS THIS A SIMULTANEOUS REQUIREMENT/ CAPABILITY
T(7) = YES ?
NO
RECORD SHORTCOMING
YES
PCB SETS ≤ TESTERS SETS
P(5) ≤ T(8) ?
NO
RECORD SHORTCOMING
YES
EXIT

PARAMETER GROUPS 72, 74, 78, 80 TESTERS 69, 75
NOTE: PCB PARAMETER GROUPS 72 AND 74 ARE
MATCHED TO TESTER GROUP 69
PCB PARAMETER GROUPS 78 AND 80 ARE
MATCHED TO TESTER GROUP 75
T69(13) — GENERAL INPUT CHARACTERISTICS
10 TESTER PARAMETERS, 3 INFORMATION
P72(5) — SERIAL SYNCHRONIZATION 5 PCB PARAMETERS
P74(5) — PARALLEL SYNCHRONIZATION 5 PCB PARAMETERS

T75(13) — GENERAL OUTPUT MEASUREMENT CHARACTERISTICS
10 TESTER PARAMETERS, 3 INFORMATION
P78(5) — SERIAL SYNCHRONIZATION OUTPUT
5 PCB PARAMETERS
P80(5) — PARALLEL SYNCHRONIZATION OUTPUT
5 PCB PARAMETERS



99231-22


PARAMETER GROUP 76
DIGITAL CHARACTERISTICS – OUTPUT LOGIC LEVELS
P76(7) – 6 PCB PARAMETERS, 1 INFORMATION
T76(6) – 6 TESTER PARAMETERS
99231-24
START
PCB LOGIC LEVEL "1" MAX ≤ TESTERS
P(1) ≤ T(1) ?
NO
RECORD SHORTCOMING
YES
TESTERS LOGIC LEVEL "1" MIN ≤ PCB'S
T(2) ≤ P(2) ?
NO
RECORD SHORTCOMING
YES
PCB LOGIC LEVEL "0" MAX ≤ TESTERS
P(3) ≤ T(3) ?
NO
RECORD SHORTCOMING
YES
TESTERS LOGIC LEVEL "0" MIN ≤ PCB'S
T(4) ≤ P(4) ?
NO
RECORD SHORTCOMING
YES
IS THIS SIMULTANEOUS REQUIREMENT/ CAPABILITY
P(6) = YES ?
NO
EXIT
YES
T(5) = YES ?
NO
RECORD SHORTCOMING
YES
PCB SETS ≤ TESTER SETS
P(7) ≤ T(6) ?
NO
RECORD SHORTCOMING
YES
EXIT

SECTION IIIB
MATCHUP OF PCB TEST REQUIREMENTS
TO AVAILABLE TESTERS

12-484

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Rev. Jan. 1971 Vendor's Name _____

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

-- C O N T E N T S --

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1.1	--- PCB SYSTEM MEMBER LIST (PCB PART NUMBER AND DESCRIPTION)	1
2.0	TESTER CANDIDATE LIST (TESTER PART NUMBER, VENDOR NAME AND TESTER NOMENCLATURE)	2
3.0	PCB TO TESTER MATCHUPS	3
4.0	TESTER SHORTCOMINGS	5
5.0	MATCHUP ANALYSIS SUMMARY	64

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 1.0 - PCB SYSTEM IDENTIFICATION

PCB SYSTEM NAME ..... COMBINED SYSTEM

PCB SYSTEM DESCRIPTION ..... SAMPLE PCBS

NUMBER OF PCB'S IN SYSTEM .. 21

SECTION 1.1 - PCB SYSTEM MEMBER LIST

PCB REFERENCE NUMBER	PCB PART NUMBER	PCB DESCRIPTION	PCB REFERENCE NUMBER	PCB PART NUMBER	PCB DESCRIPTION
P0001	1646333	ARITHMATIC REGISTER	P0002	1640302	MICRO CONTROLLER
P0003	1635918	PULSED INTERFERENCE DETECTOR	P0004	390039	DIGITAL AUTOPILOT
P0005	1650038	REED SOLOMON ENCODER	P0006	1650039	REED SOLOMON DECODER
P0007	390037	DIGITAL AUTOPILOT NO.1	P0008	D3567251	PROGRAM MEMORY
P0009	3177422	131072 BIT MEMORY	P0010	1646310	32K-16 RAM
P0011	3523201	ARITHMETIC UNIT	P0012	1635910	FILTER DOPPLER
P0013	1635884	GENERATOR,SYNC,CLOCK/TV.	P0014	1635883	CONTROL COMPUTER MESSAGE
P0015	3567221	DISCRETE FOURIER TRANSFORM	P0016	1633050	16 BIT MICROPROCESSOR
P0017	1650036	DECISION LOGIC MULTINET	P0018	390038	DIGITAL AUTOPILOT 2
P0019	1642182	MEMORY	P0020	1635972	MICROPROCESSOR
P0021	390040	DIGITAL AUTOPILOT			

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 2.0 - TESTER CANDIDATE LIST

NUMBER OF TESTER CANDIDATES .. 8

TESTER REFERENCE NUMBER	TESTER PART NUMBER	TESTER NOMENCLATURE	VENDOR NAME
T0001	L135	FUNCTIONAL BOARD TEST SYSTEM	TERADYNE
T0002	TL-8	AUTOMATIC LOGIC BOARD TESTER	TRACE INSTRUMENTS
T0003	9571A	DTS-70 DIGITAL TEST SYSTEM	HEWLETT PACKARD CO.
T0004	4000	CAPABLE	COMPUTER AUTOMATION
T0005	1795 - HD/FD	LOGIC TEST SYSTEM	GEN RAD, INC.
T0006	ATS-960	TEXAS INSTRUMENTS ATS-960	TEXAS INSTRUMENTS
T0007	3040 A	LOGIC TESTER	JOHN FLUKE MFG. CO.
T0008	1796 A	DYNAMIC DIGITAL TEST SYSYEM	GEN RAD

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 3.0 - PCB TO TESTER MATCHUPS

-- TESTER THROUGHNESS PERCENTAGE TABLE --

TESTER REFERENCE NUMBER	<--- PCB REFERENCE NUMBER --->														
	P0001	P0002	P0003	P0004	P0005	P0006	P0007	P0008	P0009	P0010	P0011	P0012	P0013	P0014	P0015
T0001	93%	91%	91%	99%	94%	94%	92%	92%	95%	90%	98%	98%	96%	98%	94%
T0002	97%	90%	93%	99%	94%	94%	99%	96%	94%	92%	96%	99%	99%	99%	99%
T0003	77%	76%	68%	93%	80%	80%	75%	77%	83%	81%	86%	86%	89%	88%	79%
T0004	96%	92%	93%	99%	94%	94%	99%	98%	96%	92%	99%	99%	99%	99%	99%
T0005	93%	93%	92%	99%	92%	91%	97%	96%	86%	87%	98%	99%	99%	99%	98%
T0006	95%	90%	83%	99%	94%	94%	90%	91%	92%	90%	99%	99%	99%	99%	93%
T0007	93%	92%	97%	99%	93%	93%	98%	97%	94%	91%	96%	99%	99%	99%	99%
T0008	95%	91%	92%	96%	90%	90%	92%	95%	89%	88%	95%	95%	96%	97%	95%

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 3.0 - PCB TO TESTER MATCHUPS * CONTINUED *

-- TESTER THROUGHNESS PERCENTAGE TABLE --

TESTER REFERENCE NUMBER	<--- PCB REFERENCE NUMBER --->					
	P0016	P0017	P0018	P0019	P0020	P0021
T0001	94%	94%	98%	96%	97%	98%
T0002	98%	96%	98%	95%	96%	97%
T0003	65%	86%	93%	74%	91%	84%
T0004	99%	95%	99%	96%	97%	96%
T0005	95%	94%	99%	92%	96%	94%
T0006	96%	97%	98%	93%	94%	95%
T0007	97%	94%	98%	97%	96%	94%
T0008	93%	91%	97%	93%	94%	94%

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
2.	P0001	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
3.	P0001	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
4.	P0001	68	1	4	1	CONDITIONAL	PULSE WIDTH
5.	P0001	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
6.	P0001	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
7.	P0001	77	1	2	1	CONDITIONAL	WORD LENGTH
8.	P0002	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
9.	P0002	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
10.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
11.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
12.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
13.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
14.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
15.	P0002	79	2	1	1	CONDITIONAL	WORD RATE

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
17.	P0003	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
18.	P0003	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
19.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
20.	P0003	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
21.	P0003	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
22.	P0003	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
23.	P0003	68	2	2	1	CONDITIONAL	CLOCK RATE MINIMUM
24.	P0003	68	2	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
25.	P0003	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
26.	P0003	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
27.	P0003	73	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
28.	P0004	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
29.	P0005	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
30.	P0005	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0005	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
32.	P0005	67	1	2	1	CONDITIONAL	ACCURACY
33.	P0005	68	1	2	2	CONDITIONAL	CLOCK RATE MINIMUM
34.	P0006	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
35.	P0006	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
36.	P0006	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
37.	P0006	67	1	2	1	CONDITIONAL	ACCURACY
38.	P0006	68	1	2	2	CONDITIONAL	CLOCK RATE MINIMUM
39.	P0007	58	1	18	1	CONDITIONAL	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC
40.	P0007	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
41.	P0007	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
42.	P0007	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
43.	P0007	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
44.	P0007	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
45.	P0007	79	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0007	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
47.	P0008	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
48.	P0008	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
49.	P0008	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
50.	P0008	77	1	2	1	CONDITIONAL	WORD LENGTH
51.	P0008	77	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
52.	P0008	79	1	2	1	CONDITIONAL	WORD LENGTH
53.	P0008	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
54.	P0008	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
55.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
56.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
57.	P0009	68	1	5	2	CONDITIONAL	RISE TIME
58.	P0009	68	1	6	2	CONDITIONAL	FALL TIME
59.	P0009	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
60.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
62.	P0010	68	1	5	2	CONDITIONAL	RISE TIME
63.	P0010	68	1	6	2	CONDITIONAL	FALL TIME
64.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
65.	P0010	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
66.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
67.	P0010	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
68.	P0010	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
69.	P0011	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
70.	P0011	64	2	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
71.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
72.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
73.	P0012	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
74.	P0012	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
75.	P0013	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0013	63	2	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
77.	P0013	63	3	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
78.	P0013	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
79.	P0014	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
80.	P0014	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
81.	P0015	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
82.	P0015	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
83.	P0015	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
84.	P0015	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
85.	P0015	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
86.	P0015	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
87.	P0015	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
88.	P0015	79	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
89.	P0016	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
90.	P0016	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
91.	P0016	67	1	2	1	CONDITIONAL	ACCURACY
92.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
93.	P0016	71	1	2	1	CONDITIONAL	WORD LENGTH
94.	P0016	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
95.	P0016	77	1	2	1	CONDITIONAL	WORD LENGTH
96.	P0017	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
97.	P0017	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
98.	P0017	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
99.	P0017	68	1	2	2	CONDITIONAL	CLOCK RATE MINIMUM
100.	P0017	71	1	2	1	CONDITIONAL	WORD LENGTH
101.	P0018	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
102.	P0018	7[illegible]	1	1	1	CONDITIONAL	WORD RATE
103.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
104.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
105.	P0019	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0001
TESTER PART NUMBER L135
TESTER NOMENCLATURE ..... FUNCTIONAL BOARD TEST SYSTEM
VENDOR NAME ..... TERADYNE
TOTAL NUMBER OF SHORTCOMINGS ... 112

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
106.	P0019	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
107.	P0020	64	1	9	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF ROM?
108.	P0020	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
109.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
110.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
111.	P0021	63	1	5	1	CONDITIONAL	MAXIMUM COUNT OF COUNTER(S) (EXPRESS DECIMALLY)
112.	P0021	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
2.	P0001	68	1	5	1	CONDITIONAL	RISE TIME
3.	P0001	68	1	6	1	CONDITIONAL	FALL TIME
4.	P0002	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
5.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
6.	P0002	68	1	5	1	CONDITIONAL	RISE TIME
7.	P0002	68	1	6	1	CONDITIONAL	FALL TIME
8.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
9.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
10.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
11.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
12.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
13.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
14.	P0003	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
15.	P0003	68	1	5	1	CONDITIONAL	RISE TIME

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	1	6	1	CONDITIONAL	FALL TIME
17.	P0003	68	2	5	1	CONDITIONAL	RISE TIME
18.	P0003	68	2	6	1	CONDITIONAL	FALL TIME
19.	P0003	73	1	1	1	CONDITIONAL	WORD RATE
20.	P0003	73	3	1	1	CONDITIONAL	WORD RATE
21.	P0003	79	1	1	1	CONDITIONAL	WORD RATE
22.	P0005	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
23.	P0005	68	1	4	1	CONDITIONAL	PULSE WIDTH
24.	P0005	68	1	6	1	CONDITIONAL	FALL TIME
25.	P0005	73	1	1	1	CONDITIONAL	WORD RATE
26.	P0005	79	1	1	1	CONDITIONAL	WORD RATE
27.	P0006	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
28.	P0006	68	1	4	1	CONDITIONAL	PULSE WIDTH
29.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
30.	P0006	73	1	1	1	CONDITIONAL	WORD RATE

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0006	79	1	1	1	CONDITIONAL	WORD RATE
32.	P0007	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
33.	P0008	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
34.	P0008	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
35.	P0008	70	1	2	1	CONDITIONAL	WORD LENGTH
36.	P0008	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
37.	P0009	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
38.	P0009	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
39.	P0009	68	1	4	1	CONDITIONAL	PULSE WIDTH
40.	P0009	68	1	6	1	CONDITIONAL	FALL TIME
41.	P0009	73	1	1	1	CONDITIONAL	WORD RATE
42.	P0009	79	1	1	1	CONDITIONAL	WORD RATE
43.	P0010	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
44.	P0010	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
45.	P0010	68	1	4	1	CONDITIONAL	PULSE WIDTH

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
47.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
48.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
49.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
50.	P0011	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
51.	P0011	58	2	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
52.	P0011	60	1	3	1	CONDITIONAL	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?
53.	P0011	60	2	3	1	CONDITIONAL	DOES PCB HAVE ASYNCHRONOUS FEEDBACK LOOPS?
54.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
55.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
56.	P0012	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
57.	P0013	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
58.	P0014	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
59.	P0015	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
60.	P0015	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0016	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
62.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
63.	P0017	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
64.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
65.	P0017	68	1	6	1	CONDITIONAL	FALL TIME
66.	P0018	60	1	1	1	CONDITIONAL	DOES PCB HAVE SYNCHRONOUS FEEDBACK LOOPS?
67.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
68.	P0019	67	1	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
69.	P0019	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
70.	P0019	68	1	4	1	CONDITIONAL	PULSE WIDTH
71.	P0019	68	1	5	1	CONDITIONAL	RISE TIME
72.	P0019	68	1	6	1	CONDITIONAL	FALL TIME
73.	P0020	67	1	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
74.	P0020	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
75.	P0020	73	1	1	1	CONDITIONAL	WORD RATE

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0002
TESTER PART NUMBER TL-8
TESTER NOMENCLATURE ..... AUTOMATIC LOGIC BOARD TESTER
VENDOR NAME ..... TRACE INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 80

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
77.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
78.	P0021	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
79.	P0021	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
80.	P0021	77	1	2	1	CONDITIONAL	WORD LENGTH

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
2.	P0001	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
3.	P0001	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
4.	P0001	68	1	4	1	CONDITIONAL	PULSE WIDTH
5.	P0001	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
6.	P0001	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
7.	P0001	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
8.	P0001	77	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)
9.	P0001	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
10.	P0002	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
11.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
12.	P0002	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
13.	P0002	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
14.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
15.	P0003	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
17.	P0003	68	2	2	1	CONDITIONAL	CLOCK RATE MINIMUM
18.	P0003	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
19.	P0003	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
20.	P0004	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
21.	P0005	67	1	2	1	CONDITIONAL	ACCURACY
22.	P0005	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
23.	P0005	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
24.	P0005	68	1	4	1	CONDITIONAL	PULSE WIDTH
25.	P0005	68	1	5	1	CONDITIONAL	RISE TIME
26.	P0005	68	1	6	1	CONDITIONAL	FALL TIME
27.	P0005	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
28.	P0005	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
29.	P0006	67	1	2	1	CONDITIONAL	ACCURACY
30.	P0006	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0006	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
32.	P0006	68	1	4	1	CONDITIONAL	PULSE WIDTH
33.	P0006	68	1	5	1	CONDITIONAL	RISE TIME
34.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
35.	P0006	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
36.	P0006	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
37.	P0007	58	1	18	1	CONDITIONAL	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC
38.	P0007	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
39.	P0007	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
40.	P0007	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
41.	P0008	58	1	24	1	CONDITIONAL	ARE THERE AN. DYNAMIC CHIPS? (NO=1,YES=2)
42.	P0008	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
43.	P0008	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
44.	P0008	77	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)
45.	P0008	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0009	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
47.	P0009	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
48.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
49.	P0009	68	1	5	1	CONDITIONAL	RISE TIME
50.	P0009	68	1	6	1	CONDITIONAL	FALL TIME
51.	P0009	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
52.	P0009	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
53.	P0010	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
54.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
55.	P0010	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
56.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
57.	P0010	68	1	4	1	CONDITIONAL	PULSE WIDTH
58.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
59.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
60.	P0010	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0010	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
62.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
63.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
64.	P0011	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
65.	P0011	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
66.	P0012	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
67.	P0012	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
68.	P0012	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
69.	P0013	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
70.	P0013	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
71.	P0013	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
72.	P0014	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
73.	P0014	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
74.	P0015	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
75.	P0015	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0015	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
77.	P0016	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
78.	P0016	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
79.	P0016	67	1	2	1	CONDITIONAL	ACCURACY
80.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
81.	P0016	71	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS)
82.	P0016	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
83.	P0016	77	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)
84.	P0016	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
85.	P0017	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
86.	P0017	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
87.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
88.	P0017	68	1	5	1	CONDITIONAL	RISE TIME
89.	P0017	68	1	6	1	CONDITIONAL	FALL TIME
90.	P0017	71	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL INPUT CHARACTERISTICS)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0003
TESTER PART NUMBER 9571A
TESTER NOMENCLATURE ..... DTS-70 DIGITAL TEST SYSTEM
VENDOR NAME ..... HEWLETT PACKARD CO.
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
91.	P0018	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
92.	P0018	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL CUTPUT CHARACTERISTICS)
93.	P0019	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
94.	P0019	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
95.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
96.	P0019	67	3	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
97.	P0019	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
98.	P0019	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
99.	P0019	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
100.	P0020	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
101.	P0020	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
102.	P0020	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)
103.	P0021	73	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - PARALLEL INPUT CHARACTERISTICS)
104.	P0021	77	0	0	0	CRITICAL	(DIGITAL CHARACTERISTICS - SERIAL OUTPUT CHARACTERISTICS)
105.	P0021	79	0	0	0	CRITICAL	(DIGITAL CHARACTERSITICS - PARALLEL OUTPUT CHARACTERISTICS)

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0004
TESTER PART NUMBER 4000
TESTER NOMENCLATURE ..... CAPABLE
VENDOR NAME ..... COMPUTER AUTOMATION
TOTAL NUMBER OF SHORTCOMINGS ... 63

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1	P0001	58	1	13	1	CONDITIONAL	NNIL
2.	P0001	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
3.	P0001	68	1	5	1	CONDITIONAL	RISE TIME
4.	P0001	68	1	6	1	CONDITIONAL	FALL TIME
5.	P0002	68	1	5	1	CONDITIONAL	RISE TIME
6.	P0002	68	1	6	1	CONDITIONAL	FALL TIME
7.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
8.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
9.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
10.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
11.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
12.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
13.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
14.	P0003	68	1	5	1	CONDITIONAL	RISE TIME
15.	P0003	68	1	6	1	CONDITIONAL	FALL TIME

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0004
TESTER PART NUMBER 4000
TESTER NOMENCLATURE ..... CAPABLE
VENDOR NAME ..... COMPUTER AUTOMATION
TOTAL NUMBER OF SHORTCOMINGS ... 63

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	2	2	1	CONDITIONAL	CLOCK RATE MINIMUM
17.	P0003	68	2	5	1	CONDITIONAL	RISE TIME
18.	P0003	68	2	6	1	CONDITIONAL	FALL TIME
19.	P0003	73	3	1	1	CONDITIONAL	WORD RATE
20.	P0003	79	1	1	1	CONDITIONAL	WORD RATE
21.	P0005	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
22.	P0005	68	1	5	1	CONDITIONAL	RISE TIME
23.	P0005	68	1	6	1	CONDITIONAL	FALL TIME
24.	P0005	73	1	1	1	CONDITIONAL	WORD RATE
25.	P0005	79	1	1	1	CONDITIONAL	WORD RATE
26.	P0006	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
27.	P0006	68	1	5	1	CONDITIONAL	RISE TIME
28.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
29.	P0006	73	1	1	1	CONDITIONAL	WORD RATE
30.	P0006	79	1	1	1	CONDITIONAL	WORD RATE

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0004
TESTER PART NUMBER 4000
TESTER NOMENCLATURE ..... CAPABLE
VENDOR NAME ..... COMPUTER AUTOMATION
TOTAL NUMBER OF SHORTCOMINGS ... 63

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0007	58	1	18	1	CONDITIONAL	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC
32.	P0008	79	1	2	1	CONDITIONAL	WORD LENGTH
33.	P0008	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
34.	P0009	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
35.	P0009	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
36.	P0009	73	1	1	1	CONDITIONAL	WORD RATE
37.	P0009	79	1	1	1	CONDITIONAL	WORD RATE
38.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
39.	P0010	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
40.	P0010	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
41.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
42.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
43.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
44.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
45.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0004
TESTER PART NUMBER 4000
TESTER NOMENCLATURE ..... CAPABLE
VENDOR NAME ..... COMPUTER AUTOMATION
TOTAL NUMBER OF SHORTCOMINGS ... 63

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
47.	P0017	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
48.	P0017	68	1	5	1	CONDITIONAL	RISE TIME
49.	P0017	68	1	6	1	CONDITIONAL	FALL TIME
50.	P0017	71	1	1	1	CONDITIONAL	DATA BIT RATE
51.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
52.	P0019	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
53.	P0019	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
54.	P0019	68	1	5	1	CONDITIONAL	RISE TIME
55.	P0019	68	1	6	1	CONDITIONAL	FALL TIME
56.	P0020	67	1	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
57.	P0020	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
58.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
59.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
60.	P0021	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER PEFERENCE NUMBER T0004
TESTER PART NUMBER 4000
TESTER NOMENCLATURE ..... CAPABLE
VENDOR NAME ..... COMPUTER AUTOMATION
TOTAL NUMBER OF SHORTCOMINGS ... 63

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0021	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
62.	P0021	77	1	1	1	CONDITIONAL	DATA BIT RATE
63.	P0021	77	1	2	1	CONDITIONAL	WORD LENGTH

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	58	1	13	1	CONDITIONAL	HNIL
2.	P0001	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
3.	P0001	68	1	4	1	CONDITIONAL	PULSE WIDTH
4.	P0001	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
5.	P0001	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
6.	P0001	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
7.	P0001	76	1	4	1	CONDITIONAL	LOGIC LEVEL "0" MINIMUM
8.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
9.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
10.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
11.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
12.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
13.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
14.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
15.	P0003	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
17.	P0003	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
18.	P0003	68	2	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
19.	P0003	73	1	1	1	CONDITIONAL	WORD RATE
20.	P0003	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
21.	P0003	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
22.	P0003	73	3	1	1	CONDITIONAL	WORD RATE
23.	P0003	73	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
24.	P0003	79	1	1	1	CONDITIONAL	WORD RATE
25.	P0004	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
26.	P0005	67	1	2	1	CONDITIONAL	ACCURACY
27.	P0005	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
28.	P0005	68	1	4	1	CONDITIONAL	PULSE WIDTH
29.	P0005	68	1	5	1	CONDITIONAL	RISE TIME
30.	P0005	68	1	6	1	CONDITIONAL	FALL TIME

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0005	73	1	1	1	CONDITIONAL	WORD RATE
32.	P0005	79	1	1	1	CONDITIONAL	WORD RATE
33.	P0006	67	1	2	1	CONDITIONAL	ACCURACY
34.	P0006	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
35.	P0006	68	1	4	1	CONDITIONAL	PULSE WIDTH
36.	P0006	68	1	5	1	CONDITIONAL	RISE TIME
37.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
38.	P0006	73	1	1	1	CONDITIONAL	WORD RATE
39.	P0006	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
40.	P0006	79	1	1	1	CONDITIONAL	WORD RATE
41.	P0007	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
42.	P0007	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
43.	P0007	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
44.	P0008	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
45.	P0008	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0008	77	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
47.	P0008	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
48.	P0009	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
49.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
50.	P0009	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
51.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
52.	P0009	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
53.	P0009	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
54.	P0009	68	1	4	1	CONDITIONAL	PULSE WIDTH
55.	P0009	68	1	5	1	CONDITIONAL	RISE TIME
56.	P0009	68	1	6	1	CONDITIONAL	FALL TIME
57.	P0009	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
58.	P0009	73	1	1	1	CONDITIONAL	WORD RATE
59.	P0009	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
60.	P0009	79	1	1	1	CONDITIONAL	WORD RATE

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... OGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0010	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
62.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
63.	P0010	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
64.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
65.	P0010	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
66.	P0010	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
67.	P0010	68	1	4	1	CONDITIONAL	PULSE WIDTH
68.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
69.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
70.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
71.	P0010	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
72.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
73.	P0011	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
74.	P0011	58	2	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
75.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
77.	P0012	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
78.	P0015	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
79.	P0015	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
80.	P0015	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
81.	P0016	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
82.	P0016	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
83.	P0016	67	1	2	1	CONDITIONAL	ACCURACY
84.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
85.	P0016	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
86.	P0016	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
87.	P0017	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
88.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
89.	P0017	68	1	5	1	CONDITIONAL	RISE TIME
90.	P0017	68	1	6	1	CONDITIONAL	FALL TIME

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
91.	P0017	71	1	1	1	CONDITIONAL	DATA BIT RATE
92.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
93.	P0019	58	1	24	1	CONDITIONAL	ARE THERE ANY DYNAMIC CHIPS? (NO=1,YES=2)
94.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
95.	P0019	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
96.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
97.	P0019	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
98.	P0019	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
99.	P0019	68	1	4	1	CONDITIONAL	PULSE WIDTH
100.	P0019	68	1	7	1	CONDITIONAL	IS CLOCK SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
101.	P0019	68	1	8	1	CONDITIONAL	HOW MANY OF THIS SET ARE REQUIRED?
102.	P0020	67	1	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
103.	P0020	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
104.	P0020	73	1	1	1	CONDITIONAL	WORD RATE
105.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFFRENCE NUMBER T0005
TESTER PART NUMBER ..... 1795 - HD/FD
TESTER NOMENCLATURE ..... LOGIC TEST SYSTEM
VENDOR NAME ..... GEN RAD, INC.
TOTAL NUMBER OF SHORTCOMINGS ... 113

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
106.	P0020	79	1	1	1	CONDITIONAL	WORD RATE
107.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
108.	P0021	58	1	17	1	CONDITIONAL	EIA
109.	P0021	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
110.	P0021	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
111.	P0021	76	1	7	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
112.	P0021	76	2	1	1	CONDITIONAL	LOGIC LEVEL "1" MAXIMUM
113.	P0021	76	2	4	1	CONDITIONAL	LOGIC LEVEL "0" MINIMUM

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	65	1	1	1	CONDITIONAL	DOES PCB HAVE MICROPROCESSORS? (NO=1 YES=2)
2.	P0001	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
3.	P0001	68	1	5	1	CONDITIONAL	RISE TIME
4.	P0001	68	1	6	1	CONDITIONAL	FALL TIME
5.	P0001	77	1	2	1	CONDITIONAL	WORD LENGTH
6.	P0002	68	1	5	1	CONDITIONAL	RISE TIME
7.	P0002	68	1	6	1	CONDITIONAL	FALL TIME
8.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
9.	P0002	73	1	2	1	CONDITIONAL	WORD LENGTH
10.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
11.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
12.	P0002	79	1	2	1	CONDITIONAL	WORD LENGTH
13.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
14.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
15.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
17.	P0003	68	1	5	1	CONDITIONAL	RISE TIME
18.	P0003	68	1	6	1	CONDITIONAL	FALL TIME
19.	P0003	68	2	2	1	CONDITIONAL	CLOCK RATE MINIMUM
20.	P0003	68	2	5	1	CONDITIONAL	RISE TIME
21.	P0003	68	2	6	1	CONDITIONAL	FALL TIME
22.	P0003	73	1	1	1	CONDITIONAL	WORD RATE
23.	P0003	73	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
24.	P0003	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
25.	P0003	73	2	2	1	CONDITIONAL	WORD LENGTH
26.	P0003	73	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
27.	P0003	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
28.	P0003	73	3	1	1	CONDITIONAL	WORD RATE
29.	P0003	73	3	2	1	CONDITIONAL	WORD LENGTH
30.	P0003	73	3	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIPEMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0003	73	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
32.	P0003	73	4	2	1	CONDITIONAL	WORD LENGTH
33.	P0003	79	1	1	1	CONDITIONAL	WORD RATE
34.	P0003	79	1	2	1	CONDITIONAL	WORD LENGTH
35.	P0003	79	2	2	1	CONDITIONAL	WORD LENGTH
36.	P0004	73	1	2	1	CONDITIONAL	WORD LENGTH
37.	P0005	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
38.	P0005	73	1	1	1	CONDITIONAL	WORD RATE
39.	P0005	73	1	2	1	CONDITIONAL	WORD LENGTH
40.	P0005	79	1	1	1	CONDITIONAL	WORD RATE
41.	P0005	79	1	2	1	CONDITIONAL	WORD LENGTH
42.	P0006	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
43.	P0006	73	1	1	1	CONDITIONAL	WORD RATE
44.	P0006	73	1	2	1	CONDITIONAL	WORD LENGTH
45.	P0006	79	1	1	1	CONDITIONAL	WORD RATE

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0006	79	1	2	1	CONDITIONAL	WORD LENGTH
47.	P0007	58	1	18	1	CONDITIONAL	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC
48.	P0007	73	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
49.	P0007	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
50.	P0007	73	2	2	1	CONDITIONAL	WORD LENGTH
51.	P0007	73	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
52.	P0007	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
53.	P0007	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
54.	P0007	79	2	2	1	CONDITIONAL	WORD LENGTH
55.	P0007	79	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
56.	P0007	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
57.	P0008	73	1	2	1	CONDITIONAL	WORD LENGTH
58.	P0008	73	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
59.	P0008	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
60.	P0008	73	2	2	1	CONDITIONAL	WORD LENGTH

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 105

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0008	73	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
62.	P0008	77	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
63.	P0008	79	1	2	1	CONDITIONAL	WORD LENGTH
64.	P0008	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
65.	P0008	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
66.	P0009	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
67.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
68.	P0009	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
69.	P0009	73	1	1	1	CONDITIONAL	WORD RATE
70.	P0009	73	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
71.	P0009	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
72.	P0009	79	1	1	1	CONDITIONAL	WORD RATE
73.	P0010	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)
74.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
75.	P0010	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
77.	P0010	73	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
78.	P0010	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET APE EXPECTED SIMULTANEOUSLY?
79.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
80.	P0010	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
81.	P0010	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
82.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
83.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
84.	P0012	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
85.	P0014	79	1	2	1	CONDITIONAL	WORD LENGTH
86.	P0015	65	1	1	1	CONDITIONAL	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)
87.	P0015	73	1	2	1	CONDITIONAL	WORD LENGTH
88.	P0015	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
89.	P0015	73	2	2	1	CONDITIONAL	WORD LENGTH
90.	P0015	73	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
91.	P0015	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
92.	P0015	79	2	2	1	CONDITIONAL	WORD LENGTH
93.	P0015	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
94.	P0015	79	3	2	1	CONDITIONAL	WORD LENGTH
95.	P0015	79	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
96.	P0016	65	1	1	1	CONDITIONAL	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)
97.	P0016	71	1	2	1	CONDITIONAL	WORD LENGTH
98.	P0016	73	1	2	1	CONDITIONAL	WORD LENGTH
99.	P0016	73	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
100.	P0016	77	1	2	1	CONDITIONAL	WORD LENGTH
101.	P0017	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
102.	P0017	71	1	2	1	CONDITIONAL	WORD LENGTH
103.	P0018	65	1	1	1	CONDITIONAL	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)
104.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
105.	P0019	64	1	12	1	CONDITIONAL	IF YES, ARE RAM DEVICES DYNAMIC? (NO=1,YES=2)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
106.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
107.	P0019	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
108.	P0019	68	1	4	1	CONDITIONAL	PULSE WIDTH
109.	P0019	68	1	5	1	CONDITIONAL	RISE TIME
110.	P0019	68	1	6	1	CONDITIONAL	FALL TIME
111.	P0019	73	1	2	1	CONDITIONAL	WORD LENGTH
112.	P0019	73	2	2	1	CONDITIONAL	WORD LENGTH
113.	P0020	65	1	1	1	CONDITIONAL	DOES PCB HAVE MICROPROCESSORS? (NO=1,YES=2)
114.	P0020	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
115.	P0020	73	1	1	1	CONDITIONAL	WORD RATE
116.	P0020	73	1	2	1	CONDITIONAL	WORD LENGTH
117.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
118.	P0020	79	1	1	1	CONDITIONAL	WORD RATE
119.	P0020	79	1	2	1	CONDITIONAL	WORD LENGTH
120.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0006
TESTER PART NUMBER ATS-960
TESTER NOMENCLATURE ..... TEXAS INSTRUMENTS ATS-960
VENDOR NAME ..... TEXAS INSTRUMENTS
TOTAL NUMBER OF SHORTCOMINGS ... 125

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
121.	P0021	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
122.	P0021	73	1	2	1	CONDITIONAL	WORD LENGTH
123.	P0021	77	1	2	1	CONDITIONAL	WORD LENGTH
124.	P0021	79	1	2	1	CONDITIONAL	WORD LENGTH
125.	P0021	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	67	1	4	1	CONDITIONAL	RIPPLE PEAK TO PEAK
2.	P0001	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
3.	P0001	68	1	3	1	CONDITIONAL	CLOCK RATE MAXIMUM
4.	P0001	68	1	4	1	CONDITIONAL	PULSE WIDTH
5.	P0001	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
6.	P0001	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
7.	P0001	76	1	4	1	CONDITIONAL	LOGIC LEVEL "0" MINIMUM
8.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
9.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
10.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
11.	P0002	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
12.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
13.	P0002	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
14.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
15.	P0002	79	2	3	1	CONDITIONAL	WORD SEQUENCE LENGTH

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
17.	P0003	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
18.	P0003	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
19.	P0003	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
20.	P0004	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
21.	P0005	67	1	2	1	CONDITIONAL	ACCURACY
22.	P0005	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
23.	P0005	68	1	4	1	CONDITIONAL	PULSE WIDTH
24.	P0005	68	1	5	1	CONDITIONAL	RISE TIME
25.	P0005	68	1	6	1	CONDITIONAL	FALL TIME
26.	P0005	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
27.	P0006	67	1	2	1	CONDITIONAL	ACCURACY
28.	P0006	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
29.	P0006	68	1	4	1	CONDITIONAL	PULSE WIDTH
30.	P0006	68	1	5	1	CONDITIONAL	RISE TIME

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
32.	P0006	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
33.	P0007	58	1	18	1	CONDITIONAL	SPECIAL EDGE CONNECTOR DRIVE/RECEIVE LOGIC
34.	P0007	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
35.	P0008	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
36.	P0008	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
37.	P0008	79	1		1	CONDITIONAL	WORD SEQUENCE LENGTH
38.	P0009	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
39.	P0009	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
40.	P0009	68	1	4	1	CONDITIONAL	PULSE WIDTH
41.	P0009	68	1	5	1	CONDITIONAL	RISE TIME
42.	P0009	68	1	6	1	CONDITIONAL	FALL TIME
43.	P0009	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
44.	P0010	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
45.	P0010	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0010	68	1	4	1	CONDITIONAL	PULSE WIDTH
47.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
48.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
49.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
50.	P0010	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
51.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
52.	P0011	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
53.	P0011	58	2	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
54.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
55.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
56.	P0011	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
57.	P0011	76	2	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
58.	P0012	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
59.	P0013	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
60.	P0014	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0015	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
62.	P0015	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
63.	P0016	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
64.	P0016	67	1	2	1	CONDITIONAL	ACCURACY
65.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
66.	P0016	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
67.	P0017	68	1	2	1	CONDITIONAL	CLOCK RATE MINIMUM
68.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
69.	P0017	68	1	5	1	CONDITIONAL	RISE TIME
70.	P0017	68	1	6	1	CONDITIONAL	FALL TIME
71.	P0017	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
72.	P0018	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
73.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
74.	P0019	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
75.	P0019	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0007
TESTER PART NUMBER ..... 3040 A
TESTER NOMENCLATURE ..... LOGIC TESTER
VENDOR NAME ..... JOHN FLUKE MFG. CO.
TOTAL NUMBER OF SHORTCOMINGS ... 87

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0019	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
77.	P0020	67	1	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
78.	P0020	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
79.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
80.	P0020	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
81.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
82.	P0021	58	1	17	1	CONDITIONAL	EIA
83.	P0021	67	2	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
84.	P0021	67	3	1	1	CONDITIONAL	POLARITIES/VOLTAGE(S)
85.	P0021	76	1	2	1	CONDITIONAL	LOGIC LEVEL "1" MINIMUM
86.	P0021	76	2	1	1	CONDITIONAL	LOGIC LEVEL "1" MAXIMUM
87.	P0021	76	2	4	1	CONDITIONAL	LOGIC LEVEL "0" MINIMUM

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
1.	P0001	58	1	13	1	CONDITIONAL	HNIL
2.	P0001	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
3.	P0001	68	1	4	1	CONDITIONAL	PULSE WIDTH
4.	P0001	73	1	2	1	CONDITIONAL	WORD LENGTH
5.	P0001	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
6.	P0002	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
7.	P0002	68	1	4	1	CONDITIONAL	PULSE WIDTH
8.	P0002	73	1	1	1	CONDITIONAL	WORD RATE
9.	P0002	73	1	2	1	CONDITIONAL	WORD LENGTH
10.	P0002	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
11.	P0002	73	2	2	1	CONDITIONAL	WORD LENGTH
12.	P0002	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
13.	P0002	79	1	1	1	CONDITIONAL	WORD RATE
14.	P0002	79	2	1	1	CONDITIONAL	WORD RATE
15.	P0003	66	1	5	1	CONDITIONAL	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
16.	P0003	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
17.	P0003	73	1	2	1	CONDITIONAL	WORD LENGTH
18.	P0003	73	2	2	1	CONDITIONAL	WORD LENGTH
19.	P0003	73	3	1	1	CONDITIONAL	WORD RATE
20.	P0003	73	3	2	1	CONDITIONAL	WORD LENGTH
21.	P0003	73	4	2	1	CONDITIONAL	WORD LENGTH
22.	P0003	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
23.	P0003	79	1	1	1	CONDITIONAL	WORD RATE
24.	P0004	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
25.	P0004	73	1	2	1	CONDITIONAL	WORD LENGTH
26.	P0004	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
27.	P0005	67	1	2	1	CONDITIONAL	ACCURACY
28.	P0005	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
29.	P0005	68	1	4	1	CONDITIONAL	PULSE WIDTH
30.	P0005	68	1	5	1	CONDITIONAL	RISE TIME

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
31.	P0005	68	1	6	1	CONDITIONAL	FALL TIME
32.	P0005	73	1	1	1	CONDITIONAL	WORD RATE
33.	P0005	73	1	2	1	CONDITIONAL	WORD LENGTH
34.	P0005	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
35.	P0005	79	1	1	1	CONDITIONAL	WORD RATE
36.	P0006	67	1	2	1	CONDITIONAL	ACCURACY
37.	P0006	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
38.	P0006	68	1	4	1	CONDITIONAL	PULSE WIDTH
39.	P0006	68	1	5	1	CONDITIONAL	RISE TIME
40.	P0006	68	1	6	1	CONDITIONAL	FALL TIME
41.	P0006	73	1	1	1	CONDITIONAL	WORD RATE
42.	P0006	73	1	2	1	CONDITIONAL	WORD LENGTH
43.	P0006	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
44.	P0006	79	1	1	1	CONDITIONAL	WORD RATE
45.	P0007	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
46.	P0007	73	1	2	1	CONDITIONAL	WORD LENGTH
47.	P0007	73	2	2	1	CONDITIONAL	WORD LENGTH
48.	P0007	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
49.	P0007	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
50.	P0007	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
51.	P0007	79	2	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
52.	P0007	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
53.	P0008	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
54.	P0008	73	1	2	1	CONDITIONAL	WORD LENGTH
55.	P0008	73	2	2	1	CONDITIONAL	WORD LENGTH
56.	P0008	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
57.	P0008	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
58.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
59.	P0009	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
60.	P0009	67	2	3	2	CONDITIONAL	MAXIMUM CURRENT DRAIN

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIPEMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
61.	P0009	68	1	4	1	CONDITIONAL	PULSE WIDTH
62.	P0009	68	1	5	1	CONDITIONAL	RISE TIME
63.	P0009	68	1	6	1	CONDITIONAL	FALL TIME
64.	P0009	73	1	1	1	CONDITIONAL	WORD RATE
65.	P0009	73	1	2	1	CONDITIONAL	WORD LENGTH
66.	P0009	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
67.	P0009	79	1	1	1	CONDITIONAL	WORD RATE
68.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
69.	P0010	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
70.	P0010	68	1	4	1	CONDITIONAL	PULSE WIDTH
71.	P0010	68	1	5	1	CONDITIONAL	RISE TIME
72.	P0010	68	1	6	1	CONDITIONAL	FALL TIME
73.	P0010	73	1	1	1	CONDITIONAL	WORD RATE
74.	P0010	73	1	2	1	CONDITIONAL	WORD LENGTH
75.	P0010	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM

P R I N T E D C I R C U I T B O A P D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
76.	P0010	79	1	1	1	CONDITIONAL	WORD RATE
77.	P0010	79	1	4	1	CONDITIONAL	IS THIS SET A SIMULTANEOUS REQUIREMENT? (NO=1,YES=2)
78.	P0010	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
79.	P0011	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
80.	P0011	58	2	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?
81.	P0011	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
82.	P0011	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
83.	P0011	73	1	2	1	CONDITIONAL	WORD LENGTH
84.	P0011	73	2	2	1	CONDITIONAL	WORD LENGTH
85.	P0011	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
86.	P0011	76	2	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
87.	P0012	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
88.	P0012	73	1	2	1	CONDITIONAL	WORD LENGTH
89.	P0012	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
90.	P0012	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
91.	P0013	66	1	4	1	CONDITIONAL	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)
92.	P0013	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
93.	P0013	73	1	2	1	CONDITIONAL	WORD LENGTH
94.	P0013	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
95.	P0014	66	1	5	1	CONDITIONAL	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)
96.	P0014	73	1	2	1	CONDITIONAL	WORD LENGTH
97.	P0014	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
98.	P0015	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
99.	P0015	73	1	2	1	CONDITIONAL	WORD LENGTH
100.	P0015	73	2	2	1	CONDITIONAL	WORD LENGTH
101.	P0015	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
102.	P0015	79	1	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
103.	P0015	79	2	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
104.	P0015	79	3	5	1	CONDITIONAL	HOW MANY OF THIS SET ARE EXPECTED SIMULTANEOUSLY?
105.	P0016	58	1	1	1	CONDITIONAL	WHAT IS THE MAXIMUM NUMBER OF I/O PINS USED?

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
106.	P0016	67	1	2	1	CONDITIONAL	ACCURACY
107.	P0016	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
108.	P0016	71	1	2	1	CONDITIONAL	WORD LENGTH
109.	P0016	73	1	2	1	CONDITIONAL	WORD LENGTH
110.	P0016	73	2	2	1	CONDITIONAL	WORD LENGTH
111.	P0016	73	3	2	1	CONDITIONAL	WORD LENGTH
112.	P0016	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
113.	P0017	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
114.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
115.	P0017	68	1	4	1	CONDITIONAL	PULSE WIDTH
116.	P0017	68	1	5	1	CONDITIONAL	RISE TIME
117.	P0017	68	1	6	1	CONDITIONAL	FALL TIME
118.	P0017	71	1	1	1	CONDITIONAL	DATA BIT RATE
119.	P0017	71	1	2	1	CONDITIONAL	WORD LENGTH
120.	P0017	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PAPAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
121.	P0018	67	1	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
122.	P0018	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
123.	P0018	79	1	1	1	CONDITIONAL	WORD RATE
124.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
125.	P0019	64	1	13	1	CONDITIONAL	WHAT IS THE MAXIMUM SIZE OF THE LARGEST RAM?
126.	P0019	67	3	3	2	CONDITIONAL	MAXIMUM CURRENT DRAIN
127.	P0019	68	1	4	1	CONDITIONAL	PULSE WIDTH
128.	P0019	73	1	2	1	CONDITIONAL	WORD LENGTH
129.	P0019	73	2	2	1	CONDITIONAL	WORD LENGTH
130.	P0019	73	3	2	1	CONDITIONAL	WORD LENGTH
131.	P0019	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
132.	P0020	67	2	3	1	CONDITIONAL	MAXIMUM CURRENT DRAIN
133.	P0020	73	1	1	1	CONDITIONAL	WORD RATE
134.	P0020	73	1	2	1	CONDITIONAL	WORD LENGTH
135.	P0020	73	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH

P R I N T E D C I R C U I T B O A R D T E S T S Y S T E M S S U R V E Y

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 4.0 - TESTER SHORTCOMINGS * CONTINUED *

TESTER REFERENCE NUMBER T0008
TESTER PART NUMBER ..... 1796 A
TESTER NOMENCLATURE ..... DYNAMIC DIGITAL TEST SYSYEM
VENDOR NAME ..... GEN RAD
TOTAL NUMBER OF SHORTCOMINGS ... 144

	PCB REFERENCE NUMBER	PARAMETER GROUP NUMBER	PCB SET NO.	PARAMETER NUMBER	TST SET NO.	SHORTCOMING SIGNIFICANCE	SHORTCOMING DESCRIPTION
136.	P0020	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
137.	P0020	76	2	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM
138.	P0020	79	1	1	1	CONDITIONAL	WORD RATE
139.	P0020	79	1	3	1	CONDITIONAL	WORD SEQUENCE LENGTH
140.	P0021	58	1	17	1	CONDITIONAL	EIA
141.	P0021	66	1	4	1	CONDITIONAL	DOES PCB HAVE PARITY GENERATOR/CHECKER? (NO=1,YES=2)
142.	P0021	66	1	5	1	CONDITIONAL	DOES PCB HAVE DIGITAL COMPARATORS? (NO=1,YES=2)
143.	P0021	73	1	2	1	CONDITIONAL	WORD LENGTH
144.	P0021	76	1	3	1	CONDITIONAL	LOGIC LEVEL "0" MAXIMUM

PRINTED CIRCUIT BOARD TEST SYSTEMS SURVEY

* * * MATCHUP OF PCB TEST REQUIREMENTS TO AVAILABLE TESTERS * * *

= PARAMETRIC LEVEL ANALYSIS =

SECTION 5.0 - MATCHUP ANALYSIS SUMMARY

TESTER REFERENCE NUMBER	RANK	TESTER THROUGHNESS PERCENTAGE	TESTER PART NUMBER	TESTER NOMENCLATURE	VENDOR NAME
T0004	1	97%	4000	CAPABLE	COMPUTER AUTOMATION
T0002	2	96%	TL-8	AUTOMATIC LOGIC BOARD TESTER	TRACE INSTRUMENTS
T0007	3	96%	3040 A	LOGIC TESTER	JOHN FLUKE MFG. CO.
T0001	4	95%	L135	FUNCTIONAL BOARD TEST SYSTEM	TERADYNE
T0005	5	95%	1795 - HD/FD	LOGIC TEST SYSTEM	GEN RAD, INC.
T0006	6	94%	ATS-960	TEXAS INSTRUMENTS ATS-960	TEXAS INSTRUMENTS
T0008	7	93%	1796 A	DYNAMIC DIGITAL TEST SYSTEM	GEN RAD
T0003	8	81%	9571A	DTS-70 DIGITAL TEST SYSTEM	HEWLETT PACKARD CO.

SECTION IIIC
TESTER EVALUATION FACTORS

Table 1 – Basic Tester Evaluation Scoring
Table 2 – Maintenance and Support Factors
Table 3 – Test System Hardware Features
Table 4 – Test Programming
Table 5 – Tester Software

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TABLE 1 – BASIC TESTER EVALUATION SCORING

Evaluation Subject	Max Rating	Bias Factor	Max Rating Times Bias	Weighing Factor
1.0 Matchup Report*	100	2.0	200	16.7%
2.0 Maintenance and Support	64	1.9	121.6	10.1%
3.0 Tester Hardware Features	89.5	2.0	178	14.9%
4.0 Test Programming	110	3.6	396	33.1%
5.0 Tester Software	53	5.7	302.1	25.2%
	316.5		1197.7	100%

NOTES: See Tables 2 through 4 for further criteria on Items 2.0 through 5.0.
*"Matchup of PCB Test Requirements to Available Testers," Attachment III, Section B

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TABLE 2 – MAINTENANCE AND SUPPORT FACTORS

Item	Description	Bias Factor	Baseline Criteria
1.	Size of Manufacturer (dollar sales volume/annum)	1	1 = < 10M, 2 = ≥10M and <30M 3 = ≥30M and ≤100M, 4 = >100M
2.	ATE Market Volume of Manufacturer (total dollar sales/annum in test systems of any type)	1	Same as Item No. 1
3.	Number of ATE Users of Manufacturers Board Test Systems (any type)	1	1 = < 10, 2 = ≥10 and < 30 3 = ≥30 and ≤100, 4 = >100
4.	Number of Static Board Testers Sold of the Type Proposed for Procurement	1	1 = < 10, 2 = ≥10 and <20 3 = ≥20 and ≤50, 4 = >50
5.	Service Support of Manufacturer	2.5	1 = Poor, 2 = Fair, 3 = Good, 4 = Excellent
6.	Warranty (including Parts, Material, and Workmanship)	1.5	1 = < 90 days, 2 = ≥90 days and <6 months 3 = ≥6 months and ≤1 year, 4 = >1 year
7.	MTBF (@ two 8 hour shifts per day)	2	Same as Item No. 6
8.	Support Equipment Required (in terms of dollars)	1	1 = > 50K, 2 = ≤50K and ≥25K, 3 = < 25K and ≥10K, 4 = < 10K
9.	Tester Self Test Features	1	Self-Test Type / Man / Semi-Auto / Auto Functional end-to-end: 0 / 0.5 / 1 Fault Detection: 1.5 / 2 / 2.5 Fault Isolation: 3 / 3.5 / 4
10.	Design Philosophy for Tester	0.5	1 = Commercial, 2 = Ruggedized, 4 = Militarized
11.	Test System Layout/User Interface	1.5	1 = Poor, 2 = Fair, 3 = Good, 4 - Excellent
12.	Procured Logistic Elements	1	0 = None, 1 = (1-3), 2 = (4-7), 3 = (8-12), 4 = ≥13
13.	Government Agency Procured Testers	1	0 = None, 1 = (1-3), 2 = (4-7), 3 = (8-12) 4 = ≥13
			Maximum Rating = 64 points

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TABLE 3 – TEST SYSTEM HARDWARE FEATURES

Item	Description	Bias Factor	Baseline Criteria
1.	Max. Number of Drivers/Sensors	1.5	1 = <240, 2 = ≥240 and <360 3 = ≥360 and ≤480, 4 = >480
2.	Can any I/O pin be switched to input/output via the resident program multiple times	6	1 = yes, 0 = no
3.	Pattern depth in one test load	1.5	1 = < 1024, 2 = ≥1024 and <2048 3 = ≥2048 and <4096, 4 = >4096
4.	Programmability of Drivers/Sensors	1.5	1 = 1 Family fixed by hardwired 2 = 2 Families fixed by hardwired 3 = 2 Families, Programmable ±15 volts 4 = More than 2 Families programmable
5.	Dynamic Testing	5	1 = yes, 0 = no
6.	Go/No-Go Test Method	2	1 = Known Good Board (KGB) 2 = Signature Analysis 3 = Stored Pattern 4 = Stored Pattern and KGB or Sig. Anal.
7.	Go/No-Go Throughput (~10,000 patterns)	2	1 = >30 sec, 2 = >10 sec, 3 = 3 sec, 4 = <3 sec
8.	Any Diagnostic Clip	1	0 = None, 2 = 1 clip only, 3 = multiple clips up to 24 pins, 4 = multiple clips up to 40 pins (if pulse catching, add 4 points)
9.	Single Pin Probe	2	0 = None, 2 = yes, if yes, add 1 for smartness, add 1 for pulse catching, add 1 for state sensitive
10.	Pin Isolation	6	1 = yes, 0 = no
11.	IEEE - 475 Bus	3	1 = yes, 0 = no
12.	Growth Potential from Simple, Static System to Dynamic Hybrid Multiple Programming Stations CPU Section Add ONS (i.e., diskette, tape, etc.)	1.5	1 = yes, 0 = no, if yes, add 2 = yes, 0 = no 1 = yes, 0 = no 1 = yes, 0 = no 1 = yes, 0 = no
13.	Test Fixture	1	1 = Poor, 2 = Fair, 3 = Good, 4 = Excellent
			Maximum Rating: 89.5 points

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TABLE 4 – TEST PROGRAMMING

Item	Description	Bias Factor	Baseline Criteria
1.	IC Modeling	1.5	Use report*, 10 points max.
2.	LSI Library	1.0	0 = None, 2 = <10, 4 = ≥10 and <20, 6 = ≥20 and <40, 8 = ≥40 and 80, 10 = ≥80
3.	Circuit Complexity	1.0	Use report, 10 points max.
4.	Circuit Modeling Convenience	0.5	Use report, 10 points max.
5.	Good Circuit Simulation	1.0	Use report, 10 points max.
6.	Fault Simulation	1.0	Use report, 10 points max.
7.	ATG Features	1.0	Use report, 10 points max.
8.	Test Program Language	1.0	2 = High/Med Level, 3 = MACRO, 5 = ATLAS
9.	Manual Programming	1.0	15 = With Simulator, 30 = Without Simulator
			Maximum Rating: 110 points

*Selection Guide for Digital Test Program Generation Systems, dated 25 Oct 78, for NOSC.

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TABLE 5 – TESTER SOFTWARE

Item	Description	Bias Factor	Baseline Criteria
1.	Operating System	1	2 = special purpose 3 = general purpose (add 1 point if general purpose and done by ATE manufacturer)
2.	Background/Foreground	2	6 = case 1: Program and test on one system 4 = case 2: Program only 2 = case 3: Test only 2 = case 4: External time share service 10 = case 5: Case 1 time shared
3.	Available Translators, Converters, etc.	0.5	0 = None, 1 = ≤2, 2 = >2 (add 4 points if D4 LASAR outputs available)
4.	Data Logging	5	0 = None, 1 = recording only, 2 = analysis
5.	On-line user aids/control	4	1 = Poor, 2 = Fair, 3 = Good, 4 = Excellent Look for: • stop on any test • recycle group • sync scope output • temporary on-line change to test • program capability • others
			Maximum Rating: 53 points

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SECTION III D
COST PERFORMANCE EVALUATION

- DFI Test System Quote Evaluation
- DFI Test System Manufacturer Quotes

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SECTION III D-1
COST PERFORMANCE EVALUATION

- Table I – DFI Test System Quote Evaluation July 1, 1979
- Table II – DFI Test System Quote Evaluation July 1, 1979 – Cost Adjustments and Performance
- Table III – DFI Test System Evaluation – Quoted System Point Rating
- Table IV – DFI Test System Relative D/PCB Test Program Costs

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TABLE I. DFI TEST SYSTEM QUOTE EVALUATION JULY 1, 1979

Hughes Aircraft Company Specification Item		Value	Point Rating	System Quote Score (See Notes) Spec Point Rating	CA[1] 4400	GR[2] 1795	HP[3] DTS-70	TER[4] L-135
3.2.1.1.1	Logic Families	> 2	I/F	2	2	2	2	2
3.2.1.1.2	Fault Isolation	Comp, IC 40P	5/C, 20/40P	25	20	25	25	25
3.2.1.1.3	Input/Output Pins Programmable Driver/Receiver	256	1/16P	16	16	14.3	16.8	13.5
3.2.1.1.4	Circuit Complexity	≥ 25K EG	1/5KEG	5	5	10	5.5	5
3.2.1.1.4.1	Test Comprehensiveness	Ability	5	5	5	5	5	5
3.2.1.1.5	Test Pattern Frequency/PIN	10K	1/2K	5	5	33	5	0.5
3.2.1.1.6	Prime Power (-) 1/% if < 5%	115 ± 5%/50-60 Hz	5	5	3	5	5	5
3.2.1.2.1.1	Mini Computer	> 12I/O chn	1/2I/O	6	8	6	7	9
	MEM	> 32KBytes	1/2KBytes	16	64	16	128	40
3.2.1.2.1.2.1	Disc Controller	2 drives	1/DR	2	2	2	1	0
	MEM	≥ 2.5 MBytes	2/MBytes	5	20	4.8	39.2	0
3.2.1.2.1.3	Mass Storage	≥ 256 KBytes	1/8KBytes	32	32	0	-	78.75
3.2.1.2.1.4	Line Printer	132 CLMN	1/2 CLM	66	66	66	66	40
		200L/M	1/10L/M	20	20	7	40	12
3.2.1.2.2.2	Drivers	L ± 15 H ± 15	1/2v $\frac{1}{2v}$	15	19	15	15	16
	(-) if > 8mv RES	8mv	1/2mv	-	-1	3.6	-	-1
	(-) if < 40 mv/μs SR	40 v/μs	1/40v/μs	-	1	1.5	-	-
	S/S	16ma	1/2ma	8	10	8	8	6
3.2.1.2.2.3	Receivers Threshold	± 15	1/2v	7.5	20	12	15	16
3.2.1.2.2.4	Digital Clock	L ± 15 H ± 15	1/2v 1/2v	15	0	15	2.5	16
	RES	8mv	1/2mv	4	-	3.6	-	-
	FREQ	≤ 2 MHz	1/MHz	2	1	8	5	5
3.2.1.2.2.5	Diagnostic Probes	40P	1/2P	20	20	0	0	12
	Current	I probe	1/I	1	1	1	1	1
3.2.1.2.3.1	Operator Terminal (CRT/Keyboard)	24L	1/2L	12	12	12	12	12
	KB	80 char/L	1/10Char	8	8	8	8	7.2

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TABLE I. DFI TEST SYSTEM QUOTE EVALUATION JULY 1, 1979 (Continued)

Hughes Aircraft Company Specification Item		Value	Point Rating	System Quote Score (See Notes) Spec Point Rating	CA[1] 4400	GR[2] 1795	HP[3] DTS-70	TER[4] L-135
3.2.1.2.3.2	Control Panel/Console	Controls	1	1	2	2	1	2
		Foot SW	1	1				
3.2.1.2.3.3	IEEE-488-1975-Bus	(Include)	1	1	1	1	1	1
3.2.1.2.4.1	Programmable Power Supplies	5v	1/2v	2.5	5	2.5	5*	6
		10A	1/A	10	10	10	10	12
		±10v	1/2v 1	10	15*	10*	10*	10*
		12A	1/A 2v	24	23.5	20	20	20
		±20v	1/2v 1	20	20	20*	20*	20*
		3A	1/A 2v	6	10	6	6	6
		±40v	1/2v 1	40	40*	40*	40*	40*
		2A	1.A 2v	4	8	10	10	10
3.2.1.2.5.1	Test Fixture	Include	2	2	2	2	2	2
3.2.1.3	Software OPERATIONAL	Include	20	20	20	20	20	20
	SIMULATOR	Include	30	30	30	30	30	30
	SELF TEST	Include	10	10	10	10	10	10
	DATA BASE Mgmt	Include	30	30	30	0	30	0
	COMPONENT	Include	10	10	10	10	10	10
	OTHER	Include	10	10	10	-	-	-
3.2.1.4.1	Environmental Conditions							
	(-) IF < 40°C, OPERATIONAL	10, 40°C	1/2°C	-	-5	-4	-	-5
	NONOPERATIONAL	-40, 65°C	1/2°C	-	-	0	-	-
3.2.1.4.2	Humidity	80%	1/2%	5	5	0	-	-15
3.2.1.5	Manuals OPERATOR	Include	5	5	5	5	5	5
	PROGRAM	Include	10	10	10	10	10	10
	SERVICE	Include	5	5	5	5	5	5
3.2.1.6	Training (2 persons)	Program	10	10	10	10	10	10
		Maint.	5	5	5	5	5	5
3.2.1.7	Installation & Acceptance Test	Inst.	5	5	5	5	5	5
		HAC Test Appr.	5	5	5	5	5	5
3.2.1.8	Transportability	Surface	5	5	5	5	5	5
	Raw Score Totals			589	556.0	523.3	687.0	554.95

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TABLE I. DFI TEST SYSTEM QUOTE EVALUATION JULY 1, 1979 (Continued)

NOTES:

[1]Computer Automation

[2]Gen Rad

[3]Hewlett Packard

[4]Teradyne

* Substituted additional power supplies and adjusted system cost accordingly.

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TABLE II. DFI TEST SYSTEM QUOTE EVALUATION
JULY 1, 1979 – COST ADJUSTMENTS AND PERFORMANCE

Value	Point Rating	CA[1]	GR[2]	HP[3]	TER[4]
System		160358	135005	116537	110000
	Option (1)	2500		2500	5500
				1000	2500
				600	40000
				2000	10400
				1500	14400
Additional PS	10v 10a	545	1090	1635	1090
Dual	0/20v 3a		622	622	622
	0/20v 3a				
Single	0/40v 5a		545	545	545
	0/40v 5a	545	545	545	545
	0/20v 10a			-1600	
	0/±25 2a			-1600	
	7v 5a		-1600		
	±20v 3a		-3300		EKN-11000
	±16v 1.6a				-4000
	-50v 0.5a				-4000
		101 Centronics LP & Printer			6400
Quoted Cost/Performance ($= \frac{\text{Adjusted System \$}}{\text{Point Score}}$)		163948	132907	124284	195002
Quoted Cost/Performance		294.87	253.98	180.9	351.38

Notes: 1 = Computer Automation, 2 = Gen Rad,
3 = Hewlett Packard, 4 = Teradyne

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TABLE III. DFI TEST SYSTEM EVALUATION –
QUOTED SYSTEM POINT RATING

- Objective System Cost $145,000
- Specification System Point Score 589 Points
- Objective Cost/Performance $\frac{145000}{589} = 246.18$
- Point Rating = $\frac{\text{Objective Cost/Performance}}{\text{Quoted Cost/Performance}} \times 100$

	CA[1]	GR[2]	HP[3]	TER[4]
Quoted Cost/ Performance	295	254	181	351
Point Rating	83	97	136	70

1 = Computer Automation
2 = Gen Rad
3 = Hewlett Packard
4 = Teradyne

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AD-A080 839 HUGHES AIRCRAFT CO FULLERTON CA GROUND SYSTEMS GROUP F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
AUG 79 DAAK40-78-C-0290
UNCLASSIFIED HAC-PR79-18-669A NL



TABLE IV. DFI TEST SYSTEM RELATIVE D/PCB TEST PROGRAM COSTS

Activity or Item	Unit	Test System Requirements	
		Teradyne L-135	Other (1)
Circuit Model	Hr	24	24
Test Generation	Hr	24	100
Test Program Generation (TPG) CPU Access Time	Hr	108*	---
Hardware Verification	Hr	100	100
Update TPG, CPU Access Time	Hr	48*	---
TOTALS		304	224
Average Program Rate	Hr/IC	6.08	4.48
Relative Program Cost	-	1.36	1

*Equivalent Hours at 25$/Hr Rate

(1) CA4400, GR1795, HP DTS-70

Estimate Conditions: D/PCB: 50 ICs SSI, MSI
Test: 95% Comprehensiveness
Fault Isolation: IC pin level

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SUBSECTION III D-2
DF1 TEST SYSTEM MANUFACTURER QUOTES

- Gen Rad
- Teradyne
- Computer Automation
- Hewlett Packard

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GenRad

P.O. Box 19500 TWX 910 595 1762
17361 Armstrong Avenue
Irvine, California 92714
714 540 9830

20 June 1979

HUGHES AIRCRAFT COMPANY
Bldg. 607/C-129
Fullerton, CA. 92634

Attention: M. K. Grinter

Reference: HAC Bid No. 79/135 M.K.G.

Dear Mr. Grinter:

GenRad Inc. is pleased to respond to Hughes Aircraft Company Bid No. 79/135 M.K.G., dated 6-6-79, with the enclosed Quotation No. 1057, for the following systems:

GenRad Model 1796-A, and GenRad Model 1795HD Digital Functional Board Test Systems.

The GenRad Model 1796-A meets or exceeds all technical specifications contained in the Technical Proposal submitted to GenRad for quotation.

The GenRad Model 1795HD meets or exceeds all technical specifications contained in the Technical Proposal submitted to GenRad for quotation, with the following two exceptions:

Section 3.2.1.1.3 - The maximum number of software programmable Driver/Sensor pins is 228. However, the 1795HD can support 480 hardware programmable Driver/Sensor pins. See Section 3.1 of the 1795HD Technical Specification submitted with this quotation.

Section 3.2.1.2.4.1. The 1795HD can not provide a voltage range of ±40V. See Section 4.1 and 4.2 of the 1795HD Technical Specification.

If you should have any questions, or if we may be of further assistance, please contact the undersigned at your convenience.

Very truly yours,

Thomas A. Varin
Systems Sales Engineer

TAV:jf
Encls.

GenRad

P O Box 19500 TWX 910-595-1762
17361 Armstrong Avenue
Irvine, California 92714
714 540-9830

QUOTATION

To: HUGHES AIRCRAFT COMPANY
Bldg. 607/C-129
Fullerton, CA 92634

Attn: M. K. Grinter

Date: 19 June 1979

Reference: GR #1057
HAC #79/135 M.K.G.

GENTLEMEN:

We solicit your purchase order on the basis of the following information:

Item	Quantity	Catalog Number	Description	Unit Price	Total Price	Estimated Shipment*
1.	1	1795HD	DIGITAL PRINTED CIRCUIT BOARD TEST SYSTEM. Basic system includes the following: 1) PDP8/A with 32K memory 2) Dual DEC RK8E Disk Drive and Controller 3) Single oppy Disk Drive and Controller 4) ASR 33 Teletypewriter 5) TEC Video Terminal 6) Control Panel 7) 4 Bay Cabinet 8) 228 Programmable Driver Sensor Pins 9) GR Pulse Catching Probe 10) Diagnostic Resolution Module 11) IEEE 488 Bus Interface	$135,005.00		

Prices and Shipment F.O.B. Factory, Concord, Massachusetts

Terms (subject to credit approval): 40% with purchase order, 40% upon shipment, 20% net 30 days from installation.

Payable at par in New York or Boston funds.

Minimum billing $25 except for repair parts and cash-with-order transactions.

Quotation subject to submission of your purchase order within 30 days.

Unless otherwise stated, warranties are those published in our current product documentation.

Unless specifically marked for export, it is understood that this is a domestic quotation and that the purchased equipment is intended for use within the United States or its territories.

Stenographic and clerical errors are subject to correction.

Whether or not separately itemized above, prices shown will be increased by the amount of any applicable federal, state, or local tax that may be imposed on or because of this transaction.

Determination of prices, terms and conditions of sale and acceptance of orders are made only at general office, Concord, Massachusetts.

A surcharge will be imposed for source inspection.

*Shipping estimates are subject to revision at time of acceptance of order because of prior sales and conditions beyond our control.

GenRad, Inc.

By _____

Form 86-K/TSD

GenRad

P.O. Box 19500 TWX 910 595 1762
17361 Armstrong Avenue
Irvine, California 92714
714 540-9830

QUOTATION

To: HUGHES AIRCRAFT COMPANY
Fullerton, Ca.

Page 2 of 3

Date 19 June 1979

Reference: GR #1057
HAC #79/135 M.K.G.

GENTLEMEN:
We solicit your purchase order on the basis of the following information:

Item	Quantity	Catalog Number	Description	Unit Price	Total Price	Estimated Shipment*
			12) Single 5V 10A Fixed Supply			
			13) Triple Power Supply			
			a) 0.5 to 7.0 V @ 5A			
			b) 0.5 to 20 V @ 1.5A			
			c) 0.5 to 20 V @ 1/5A			
			14) Centronics 103 Line Printer			
			15) Caps 1X with APG CINCL One Additional Disk			
			16) Test 1X Software with 3 Disks			
			17) Assurance Adaptor			
			18) Instruction Manuals (Openation, Programming, Service, Drawings)			
			19) Operation and Programming Training for Two People			

Prices and Shipment F.O.B. Factory, Concord, Massachusetts

Terms (subject to credit approval): 40% with purchase order, 40% upon shipment, 20% net 30 days from installation.
Payable at par in New York or Boston funds.
Minimum billing $25 except for repair parts and cash-with-order transactions.
Quotation subject to submission of your purchase order within 30 days.
Unless otherwise stated, warranties are those published in our current product documentation.
Unless specifically marked for export, it is understood that this is a domestic quotation and that the purchased equipment is intended for use within the United States or its territories.

Stenographic and clerical errors are subject to correction.
Whether or not separately itemized above, prices shown will be increased by the amount of any applicable federal, state, or local tax that may be imposed on or because of this transaction.
Determination of prices, terms and conditions of sale and acceptance of orders are made only at general office, Concord, Massachusetts.
A surcharge will be imposed for source inspection.
*Shipping estimates are subject to revision at time of acceptance of order because of prior sales and conditions beyond our control.

GenRad, Inc.

By _____

Form 86-K/TSD

GenRad

P O Box 19500 TWX 910 595 1762
17361 Armstrong Avenue
Irvine, California 92714
714 540-9830

QUOTATION

To:
HUGHES AIRCRAFT COMPANY
Fullerton, CA.

Page 3 of 3

Date: 19 June 1979

Reference: GR #1057
HAC #79/135 M.K.G.

GENTLEMEN:
We solicit your purchase order on the basis of the following information:

Item	Quantity	Catalog Number	Description	Unit Price	Total Price	Estimated Shipment*

ADDITIONAL TERMS AND CONDITIONS:

Hughes agrees to use reasonable effort to confine the use of these CAPS (Computer Aided Programming Software) programs to those of its employees who are directly concerned with the operation of the GenRad, Inc., 1795 Programming Station and to advise all persons who use these programs that they contain information proprietary to GenRad, Inc. which is not to be disclosed to any other persons, and that the copying of the programs, except for Hughes' own use is prohibited.

SOFTWARE LICENSE:

A portion of the software supplied by GenRad, Inc. as a component of a system or as a separate item is furnished under a license for use of a single CPU and can be copied (with the inclusion of copyright notice) only for use on such CPU.

Prices and Shipment F.O.B. Factory, Concord, Massachusetts

Terms (subject to credit approval): 40% with purchase order, 40% upon shipment, 20% net 30 days from installation.
Payable at par in New York or Boston funds.
Minimum billing $25 except for repair parts and cash-with-order transactions.
Quotation subject to submission of your purchase order within 30 days.
Unless otherwise stated, warranties are those published in our current product documentation.
Unless specifically marked for export, it is understood that this is a domestic quotation and that the purchased equipment is intended for use within the United States or its territories.

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Determination of prices, terms and conditions of sale and acceptance of orders are made only at general office, Concord, Massachusetts.
A surcharge will be imposed for source inspection.
*Shipping estimates are subject to revision at time of acceptance of order because of prior sales and conditions beyond our control.

GenRad, Inc.

By Thomas Varin
Tom Varin
Systems Engineer

Form 86-K/TSD

4 (5 BLANK)

TERADYNE

QUOTATION

183 ESSEX STREET, BOSTON, MASSACHUSETTS 02111
TELEPHONE 617 / 482-2700, TWX 710-321-1055, CABLE TERADYNEB

No. 30416 IN REPLY PLEASE REFER TO THIS NO.

VALID FOR 60 DAYS FROM June 19, 1979

TO Hughes Aircraft Company
Post Office Box 3310
Fullerton, CA 92634

FROM Teradyne, Inc.
666 Baker
Suite 211
Costa Mesa, CA 92626

WE ARE PLEASED TO QUOTE IN REPLY TO YOUR INQUIRY:

R F Q NO	DATE OF INQUIRY	BUYER	SALESMAN	PAGE
79/135 M.K.G.	6/6/79	M. K. Grinter	Bill McCusker	1 OF 3

ITEM NO.	QUANTITY	DESCRIPTION	APPROX DELIVERY WEEKS A.R.O.	UNIT PRICE	TOTAL
1	1	L135C LSI Board Test System for LSI Boards, including the following:		$110,000	$110,000
	1	M365-53 Computing controller wired for 256K of memory			
	5	380-116 16K memory page for computing controller 80K total			
	1	H920-00 Flexible disk unit			
	4	502-047-00 10 pack double density diskettes			
	1	M367-01 CRT display and keyboard terminal			
	1	404-532-05 KSR43 Teletype teleprinter			
	1	M654 AC/DC power kiosk			
	1	M655 Power kiosk containing:			
		(1) H035 AC power controller			
	1	M656 L135 Measurement kiosk containing:			
		(1) M398-01 Measurement function bay with one-line diagnosing display			
		(1) M392 Driver-detector bay wired for 228 I/O pins			

PLEASE READ CONDITIONS OF THIS QUOTATION ON REVERSE SIDE

Rev 1 78 F483A

THANK YOU FOR THIS OPPORTUNITY TO QUOTE.

TERADYNE, INC.

DIVISION: _____

6 BY Bill McCusker

TERADYNE

QUOTATION

183 ESSEX STREET, BOSTON, MASSACHUSETTS 02111
TELEPHONE 617 / 482-2700, TWX 710-321-1055, CABLE TERADYNEB

No. 30416

IN REPLY PLEASE REFER TO THIS NO.

VALID FOR 60 DAYS FROM June 19, 1979

TO

FROM

WE ARE PLEASED TO QUOTE IN REPLY TO YOUR INQUIRY:

R.F.Q. NO.	DATE OF INQUIRY	BUYER	SALESMAN	PAGE
				2 OF 3

ITEM NO.	QUANTITY	DESCRIPTION	APPROX. DELIVERY WEEKS A.R.O.	UNIT PRICE	TOTAL
		(6) M390-60 A driver comparators, 36 pins			
		(2) M392-66 6 clock rate A, B drivers with time measurement modules, 12 pins			
		(1) M392-10 clock rate control package			
		(1) M492-10 B driver control circuitry			
		(1) M492 power bay			
		(1) M492-20 ±6V @ 6A programmable DC source			
	1	M398-60 Digital voltmeter			
	1	854-211-00 Digital guided probe			
	3	859-350-00 Interface board			
	1	854-016-00 Interface board storage box			
	1	ES135 Executive system software			
		10-year warranty			
2	3	380-116-00 16K memory page		$ 4,800	$ 14,400
3	1	404-613-05 2260 Dataproducts lineprinter with interface for M365C/CX		11,700	11,700
4	15	M390-60 A driver-comparators		1,300	19,500
5	20	M390-61 A driver-comparators and B drivers		2,000	40,000

PLEASE READ CONDITIONS OF THIS QUOTATION ON REVERSE SIDE

Rev 1/78 F483B

THANK YOU FOR THIS OPPORTUNITY TO QUOTE.

TERADYNE, INC.

DIVISION: _____

BY _____

TERADYNE

183 ESSEX STREET, BOSTON, MASSACHUSETTS 02111
TELEPHONE 617 / 482-2700, TWX 710-321-1055, CABLE TERADYNEB

QUOTATION

No. 30416 IN REPLY PLEASE REFER TO THIS NO.

VALID FOR 60 DAYS FROM June 19, 1979

TO

FROM

WE ARE PLEASED TO QUOTE IN REPLY TO YOUR INQUIRY:

R.F.Q. NO	DATE OF INQUIRY	BUYER	SALESMAN	PAGE
				3 OF 3

ITEM NO.	QUANTITY	DESCRIPTION	APPROX DELIVERY WEEKS ARO	UNIT PRICE	TOTAL
6	1	M657 Pin expansion kiosk including: (1) M392 Driver comparator bay wired for additional 228 I/0 pins (1) M492 power bay (1) 859-351-00 Interface board for pins 229-456		$ 25,000	$ 25,000
7	2	M492-21 ±16V to ±1.6A with current monitoring		2,000	4,000
8	1	M492-22 +50V to 0.5A with current monitoring		2,000	2,000
9	1	M492-23 -50V to 0.5A with current monitoring		2,000	2,000
10	1	M676 Electronic knife		11,000	11,000
11	1	M658 IEEE Bus kiosk containing: (1) H884 General purpose interface (1) H885 digital interface (1) H780 Matrix connector panel (1) H045 AC power control		5,500	5,500
12	1	H396-20 Fault injector		2,500	2,500
		NOTE: Spares should be ordered with the system - approximate price is 10% of total cost.			

PLEASE READ CONDITIONS OF THIS QUOTATION ON REVERSE SIDE

Rev 1/78 F483B

THANK YOU FOR THIS OPPORTUNITY TO QUOTE.

TERADYNE, INC.

DIVISION: _____

8 BY _____

TERADYNE INC
SUITE 211
800 BAKER STREET
COSTA MESA CALIFORNIA 92626
TELEPHONE 714 979 4590
TWX 910 595 1909

EXCEPTIONS TO HUGHES' RFQ 79/135 MKC

1. 3.2.1.1.6.1
   Change 115 volts ± 5% to 200-240 volts, single phase, 50 amps.

2. 3.2.1.2.1.2
   Delete (no discs)

3. 3.2.1.2.1.2.1
   Delete (no discs)

4) 3.2.1.2.2.2
5) 4 = Voltage resolution = 10mV
   5 = Current source: = change 16mA to 12mA

6. 3.2.1.2.2.3
   Voltage resolution = 10mV

7. 3.2.1.2.2.4
   Voltage resolution = 10mV

8. 3.2.1.2.3.1
   Change 80 characters per line to 72

9. 3.2.1.2.4.1 - 3.2.1.2.4.2
   Select 5 programmable PS from the following standard supplies available (no fixed supplies are offered).

SPECIFICATIONS FOR DC POWER SOURCES

Performance indicated applies at the interface board on the test bed.

Voltage			Current			
Range	Accuracy[1]	Programming Resolution	Current Available	Monitored Current Measurement Accuracy[1]	Resolution	Programmable Current Limits
−6 V to +6 V	0.25% + 5 mV	10 mV	6 A	0.75% + 20 mA	10 mA	0.6 A, 1.6 A, (3 + V/2)A
−16 V to +16 V	0.25% + 5 mV	10 mV	1.6 A	0.75% + 2 mA	1 mA	0.16 A, 0.6 A, 1.6 A
0 to +50 V	0.25% + 50 mV	100 mV	0.5 A	0.75% + 2 mA	1 mA	0.06 A, 0.16 A, 0.5 A
0 to −50 V	0.25% + 50 mV	100 mV	0.5 A	0.75% + 2 mA	1 mA	0.06 A, 0.16 A, 0.5 A

10. 3.2.1.4.1
    Temperature range is +10 to +30°C.

11. 3.2.1.4.2
Humidity range is 20% to 50%.

12. Section 3.2.1.2.2.4 specifies digital clocks of 2MHz frequency. The hi speed (5MHz) option has been quoted and 12 hi speed channels included.

ComputerAutomation
Industrial Products Division

QUOTATION

In reply please refer to this Quote Number.	MAC 0679002

QUOTE DATE: June 14, 1979

PLEASE MAKE PURCHASE ORDER TO:
Computer Automation
Industrial Products Division
2181 Dupont Drive, Irvine California 92713
Telephone 714 833 8830 TWX 910 595 2543

To: HUGHES AIRCRAFT
P.O. Box 3310
Fullerton, CA 92634

Attn: M.K. Grinter

Your Reference	Terms	Delivery	Quote Firm For
RFQ # 79/135 M.K.G.	NET 30 DAYS	60-90 days aro	90 days

Item No.	Quantity	Model Number	Description	Unit Price	Total Price
1	1	4400	CAPABLE Automatic Test System To include: * LSI-2 Computer with 128K Bytes Memory * Alphanumeric CRT/Keyboard * Single Flexible Disk Drive * Dual C.D.C. Moving Head Disk Drive (10M Byte) * Operator Control Panel with footswitch * Line Printer System (200 LPM) * ALL Capability * Eight UUT Interface Pin Module-ALL (256 ALL pins) * Guided Fault Isolation Clip/Probe * Advanced Fault Resolution * Powers Supplies (fully software programmable) one 0-10 Volt at 10 Amps Two 0-20 Volt at 5 Amps one 0-20 Volt at 13.5 Amps one 0-40 Volt at 3 Amps		$160,358.00

Thank you,
COMPUTER AUTOMATION, INC.
Industrial Products Division

BY _____

FORM 78248

THIS QUOTATION IS SUBJECT TO THE TERMS AND CONDITIONS ON THE REVERSE SIDE
White – Customer Copy Green – Salesman Copy Canary – Regional Office Copy Pink – Customer File Copy

ComputerAutomation
Industrial Products Division

QUOTATION

In reply please refer to this Quote Number.	MAC 0679002

QUOTE DATE: June 14, 1979

PLEASE MAKE PURCHASE ORDER TO:

Computer Automation
Industrial Products Division
2181 Dupont Drive, Irvine, California 92713
Telephone 714 833 8830 TWX 910 595 2543

To: HUGHES AIRCRAFT

Your Reference	Terms	Delivery	Quote Firm For
RFQ # 79/135 M.K.G.	NET 30 DAYS		

Item No.	Quantity	Model Number	Description	Unit Price	Total Price
			* Blank UUT Adapter Panel * Adsim Logic Simulation Capability * Full one year on-site service warranty * On-site System installation * Maintenance training for two people * Unlimited Operating and Programming training for any number of people at any time * System Self-Tests * Manuals Operation Programming Service		
			OPTIONAL ITEM:		
2	1	4717	IEEE Bus Interface	$2,500.00	

Thank you,
COMPUTER AUTOMATION, INC.
Industrial Products Division
BY

FORM 78248

THIS QUOTATION IS SUBJECT TO THE TERMS AND CONDITIONS ON THE REVERSE SIDE
White – Customer Copy Green – Salesman Copy Canary – Regional Office Copy Pink – Customer File Copy

DIGITAL PRINTED CIRCUIT BOARD

TEST PROPOSAL

prepared for

HUGHES AIRCRAFT

by

Computer Automation, Inc.

1.0 SCOPE

This proposal outlines a digital printed circuit board test system, hereafter referred to as the System.

2.0 APPLICABLE DOCUMENTS

a. CAPABLE 4400 Automatic Test System
b. CAPABLE 4180 Advanced Fault Resolution
c. CAPABLE 4000 UUT Interface Module
d. CAPABLE 4850 Simulation Capability
e. CAPABLE 4912 Real-Time Capability
f. CAPABLE 4000 Physical Installation Application Note
g. CAPABLE 4000 Series Peripherals
h. CAPABLE 4701 Analog Matrix Module
i. CAPABLE 4707 Analog Capability
j. CAPABLE 4000 UUT Power Supplies

3.0 REQUIREMENTS

3.1 System Definition

The system has equipment that is designed to provide stimulus and measurement testing capabilities for a digital printed circuit board in a production test environment. The system has the capability to test, analyze, evaluate and fault isolate the functional parameters of a digital printed circuit board or other related digital printed electronics modules.
(Ref: CAPABLE 4400 Automatic Test System)

3.2 Characteristics

3.2.1 Performance

The system meets or exceeds the following performance specifications.

3.2.1.1 System Performance Characteristics

3.2.1.1.1 Logic Families

The system has the capability to test two mixed logic families on a UUT, where both logic families appear at the edge connector. UUT's containing more than two logic families may be tested providing only two logic families appear at the edge connector. For each logic family four parameters are required:

Drive High Voltage
Drive Low Voltage
Sense High Voltage
Sense Low Voltage

3.2.1.1.1 (cont.)

Because each logic family has "dual threshold detection", high responses from the UUT which are not quite a valid high and low responses which are not quite a valid low can be isolated, thus resulting in a more thorough, more comprehensive test of the UUT. (Ref: CAPABLE 4000 Unit-Under-Test Interface Module)

3.2.1.1.2 Fault Isolation

The system has the capability to fault isolate a digital PCB to a component or an IC with any number of pins. This is accomplished by the computer guided probe and guided clip in conjunction with AFR (Advanced Fault Resolution). (Ref: CAPABLE 4180 Advanced Fault Resolution)

3.2.1.1.3 Input/Output Pins

The system has 256 input/output pins. (Ref: CAPABLE 4000 Unit-Under-Test Interface Module)

3.2.1.1.4 Circuit Complexity

The system has the capability to easily test a digital circuit board with a circuit complexity greater than 25,000 equivalent gates. This is due to the powerful processor with a large amount of main memory and disk storage that is utilized.

3.2.1.1.4.1 Test Comprehensiveness

The system has the capability of grading the test program comprehensiveness using the digital fault simulation feature. (Ref: CAPABLE 4850 Simulation Capability)

3.2.1.1.5 Test Pattern Frequency

The test system can stimulate a single pin at a frequency of 1 MHz. When several pins or all pins have their states altered from test step to test step these changes occur at approximately a 10 KHz - 50 KHz rate.

Should a faster frequency be required, as with many of the modern microprocessor based LSI boards, the real time option (Ref: CAPABLE 4912 Real-Time Capability) may be retrofitted at a later date to allow testing at up to 2 MHz across the entire pattern width. This real time or "high speed" capability is accomplished by preloading into either 1 K or 4 K deep RAMS both the patterns to be applied to the UUT and the expected responses for each test step. These inputs are then

3.2.1.1.5 (cont.) strobed into the UUT and the outputs are captured from the UUT "on the fly" at specific times under the control of 8 separate programmable clocks. If required, these inputs and outputs can be strobed to and from the UUT in synchronization with an on-board oscillator or clock generator. These high speed pins can be intermixed with static pins as specified in the RFQ.

3.2.1.1.6 Prime Power

AC Power

The system requires 50 or 60 cycle, single phase, 120 VAC + - 10 percent power. The AC should be regulated to within 3 percent under varying line conditions. (Ref: CAPABLE 4000 Physical Installation Applications Note)

3.2.1.2 Functional Subsystem

The system consists of five subsystems:

Minicomputer and Peripherals Subsystem
Digital Test Subsystem
Control and Display Subsystem
Power Supply Subsystem
UUT Connection Subsystem

3.2.1.2.1 Minicomputer and Peripherals Subsystem

3.2.1.2.1.1 Minicomputer

The minicomputer used is the powerful Computer Automation LSI 2-20 16 bit minicomputer with 128K Bytes of main memory. This processor is far in excess of that specified in the RFQ but it is felt that the overall system capability and speed can be enhanced considerably for the minimal incremental cost of the additional hardware.

Using a computer with a smaller word length or less main memory would generally require more disk accesses (to external memory) for a given operation, hence, a slower time of execution.

3.2.1.2.1.2 Disk Controller

The disk controller interfaces with a single computer I/O channel. It receives commands from the computer and controls data transfers between the computer and the disk units according to the computer command.

3.2.1.2.1.2.1 Disk Units

The system contains a Control Data Corporation dual disk drive unit with a combined capacity of 10 Megabytes. Again, this capacity is twice that requested in the RFQ, but as boards become more and more complex this additional capacity is needed for storage of large simulation and fault isolation.

3.2.1.2.1.3 Mass Storage

The system contains a single floppy disk drive with 256 K byte storage capacity. This drive is used primarily to receive software updates and for data storage. In an emergency, the system can execute from the floppy disk in all modes except logic simulation. This includes program entry, edit, debug, execution and fault isolation. (Ref: CAPABLE 4000 Series System Peripherals)

3.2.1.2.1.4 Line Printer

The system contains a full line printer (not a character printer) that can print out program listings and reports in 132 columns at a minimum rate of 200 lines per minute. Ref: CAPABLE 4000 Series System Peripherals)

3.2.1.2.2 Digital Test System

3.2.1.2.2.1 Programmable Logic Driver/Receiver

The system contain 256 software programmable logic driver/receiver pins. Each logic family can be independently programmed over a range of + - 18 Volts on drive and + - 20 Volts on receive. (Ref: CAPABLE 4000 Unit-Under-Test Interface Module)

3.2.1.2.2.2 Drivers

The system contains drivers with the following specifications:

Logic "Low" Voltage Range: -18V to +18V

Logic "High" Voltage Range: -20V to +20

Static Accuracy: + - 30 MV + - .5 of programmed value

Voltage Resolution: 10 MV

Slew Rate: 80 Volts/microsecond

Current Source: 20 MA

Current Sink: 20 MA

3.2.1.2.1.2.1 Disk Units

The system contains a Control Data Corporation dual disk drive unit with a combined capacity of 10 Megabytes. Again, this capacity is twice that requested in the RFQ, but as boards become more and more complex this additional capacity is needed for storage of large simulation and fault isolation.

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Static Accuracy: + - 30 MV + - .5 of programmed value

Voltage Resolution: 10 MV

Slew Rate: 80 Volts/microsecond

Current Source: 20 MA

Current Sink: 20 MA

3.2.1.2.2.3 Receivers

The system provides receivers with the following specifications:

"High" Threshold Range: + - 20 Volts

"Low" Threshold Range: + - 20 Volts

Static Accuracy: + - 30 MV + - .5% of programmed value

Input Impedance: 1 Mohn typical; 50 pF at motherboard connector

Short Circuit Protection: + - 80 V maximum, indefinitely

3.2.1.2.2.4 Digital Clock

The system has the ability to clock a pin at a rate of approximately 1 MHz for a specific number of pulses or continuously until interrupted by the operator. All other drivers specifications apply to the pin.

If a faster clocking frequency is desired, by addition of the CAPABLE 4912 Real-Time Option, one or more pins can be stimulated at up to 20 MHz using the RZM and RlM features.

3.2.1.2.2.5 Diagnostic Probes

The system has a diagnostic computer guided probe and guided clip to aid the operator in troubleshooting a defective UUT and isolating the cause of failure to a bad component of IC. The system contains a 16 pin clip (usable on IC's of up to 16 pins) and a 24 pin clip (usable on IC's up to 40 pins). The Advanced Fault Resolution feature (Ref: CAPABLE 4180 Advanced Fault Resolution) provides a current sensing probe to enhance the systems fault isolation capability.

3.2.1.2.3 Control and Display Subsystem

3.2.1.2.3.1 Operator Terminal (CRT/Keyboard)

The system has a CRT terminal with keyboard and internal memory for displa of up to 24 lines of text at 80 characters per line.

Control Panel/Console

The system has a control panel/console that is designed to contain all the controls and indicators necessary for troubleshooting and testing the UUT. The control panel/console also provides the use of a footswitch for hands-free operation during testing.

3.2.1.3.3 IEEE 488 - 1975 Bus (Optional)

Quoted as an option is the IEEE Bus and controlling software. With this option the system can be expanded, via the addition of IEEE Bus controlled instruments, to allow for analog testing. With the addition of the 4701 Analog Matrix Module (Ref: CAPABLE 4701 Analog Matrix Module) these instruments can be routed to selected pins at the UUT under software control. By this addition of the 4707 Analog Capability (Ref: CAPABLE 4707 Analog Capability) several additional instruments can be installed, multiplexed onto 5 or 10 system busses and then demultiplexed onto the selected UUT pin (through the 4701 Analog Matrix Module). At this point the system would be a true hybrid tester, capable of testing digital, analog or hybrid circuit modules.

3.2.1.2.4 Power Supply Subsystem

3.2.1.2.4.1 Programmable Power Supplies

The system has four software programmable power supplies with the following specifications: (Ref: CAPABLE 4000 Unit-Under-Test Power Supplies)

	1	2	3	4	Unit
Voltage Range:	0-20	0-20	0-20	0-40	Volts
Voltage Resolution:	10	10	10	10	Millivolt
Voltage Accuracy:	0.1%	0.1%	0.1%	0.1%	of FS Range
Current Range **:	13.5	5	5	3	Amps

**Current limits are manually adjustable on these supplies

3.2.1.2.4.2 Fixed Power Supply

The system contains one fully software programmable power supply in lieu of the requested fixed power supply. The power supply has a voltage range of 0-10 Volts, a current rating of 10 Amps, a voltage resolution of 10 millivolts and a voltage accuracy of 0.1% of full scale range.

3.2.1.2.5 UUT Connection Subsystem

3.2.1.2.5.1 Test Fixture

The system contains a blank adapter panel. In order to interface a UUT for testing the user must mount his unique connector onto the blank adapter panel and wire one-for-one from the pins on the buffer card chassis mother board to your connector.

3.2.1.2.5.2 Universal Fixture

If desired a completely universal "bed of nails" test fixture can be provided. In addition, Computer Automation will prewire this fixture for up to 700 points.

3.2.1.3 Software

The following software packages are provided:

a. Operational Software
b. Digital Logic Simulator (Ref: CAPABLE 4850 Simulation Capability)
c. Systems Self Test
d. Computer and Peripherals Self-Test
e. Data Base Management System
f. Components Library

3.2.1.4 Environmental Conditions

(Ref: CAPABLE 4000 Physical Installation Application Note)

3.2.1.4.1 Temperature

The system shall withstand the effects of ambient air temperature as follows:

a. Operating Temperature
The system shall operate without degraded performance at any temperature between + 10 degrees C and + 30 degrees C.

b. Non-Operating Temperature
The system after exposure to a non-operating temperature of - 40 degrees C and + 65 degrees C shall operate without degraded performan when restored to the normal operating temperature range.

3.2.1.4.2 Humidity

The system shall maintain specified performance when exposed to relative humidity of up to 90 % (non-condensing) for continuous and intermittent periods.

3.2.1.5 Manuals

The following manuals will be provided with th system:

a. Operating
b. Programming
c. Service

3.2.1.6 Training

The following training courses are provided at the manufacturing facility in Irvine, California.

a. Tester Operating and Programming
b. Tester Maintenance

NOTE: The Operating and Programming training courses will be held for any number of people at any time during the lifetime of system ownership. This is truly unlimited training at no cost. Maintenance training is limited to two (2) persons. Additional maintenance training credits are available at a nominal cost.

3.2.1.7 Installation and Acceptance Test

System installation will be performed by Computer Automation personnel and the series of system self-checks will be run. These self-checks will be the basis for system acceptance. No later than 30 days prior to shipment Computer Automation will provide to Hughes Aircraft copies of these test procedures for review and study.

3.2.1.8 Transportability

The system is capable of being trapsorted by highway, rail, water or air. Since Computer Automation is located approximately 20 miles from the Hughes facility, it is recommended that a HAC truck be utilized as the transportation medium.

HEWLETT hp PACKARD

NEELY SALES REGION · 1430 East Orangethorpe Avenue, Fullerton, California 92631 · Telephone 714 870-1000

June 12, 1979

Mr. Al Lee
Mr. John Romanelli
Mr. Mike Grinter
HUGHES AIRCRAFT COMPANY
P. O. Box 3310
Fullerton, CA 92634

Dear Gentlemen:

Attached you will find a budgetary quotation for a Hewlett-Packard Digital Board Test System. We have configured the system to meet your specifications, dated May 21, 1979, in reply to your HUGHES RFQ #79/135 MKG.

We have configured the system in two basic parts; the computer and test hardware. The following is a summary of the approximate cost:

HP 1000 Computer System	=	$ 60,300
HP 9571 Test System	=	75,785
TOTAL	=	$136,085

Because of the power of the HP 1000 RTE System, we have included a second CRT terminal so that you can do programming and data base management while you simultaneously test boards. We also included a high speed line printer to meet your data base management needs.

A complete package of software and lots of training and systems engineering consulting was also included. Since Hughes has already purchased ATLAS from Hewlett-Packard, you can simply duplicate this software. The only additional cost would be training on ATLAS at Hewlett-Packard.

We would also like to point out that Hewlett-Packard and Hughes Aircraft have both a test equipment and computer purchase agreement currently in effect. This will make a significant difference in the list prices stated above. Below is a summary of the price you will actually pay:

VOLUME END USER

HP 9571 Test System	=	$ 72,753 (4% Discount)
HP 1000 Computer System	=	47,901 (23% Discount)
TOTAL	=	$120,654

OEM SCHEDULE

HP 9571 Test System	=	$ 72,753 (4% Discount)
HP 1000 Computer System	=	43,784 (28/38% Discount)
TOTAL	=	$116,537

We look forward to meeting with you to answer any remaining questions you might have.

Sincerely,

HEWLETT-PACKARD COMPANY
Neely Sales Region

Rodger Tracy
Field Engineer, Instruments

Greg Free
Board Test Sales

Frank Rich
Field Engineer, Computer Systems

RT/GF/FR: jcp

Enclosures

BUDGETARY QUOTATION FOR HUGHES AIRCRAFT COMPANY/FULLERTON

Quantity	Item	Description	Unit Price	Total
01	HP 9571	Digital PCB Production Test Station Consisting of:	$47,000.00	$47,000.00
01		Testaid Software		
01		Fastrace Software		
01		Digital Test Unit 12 Card Slots		
02		Test Station Cabinets		
01		Test Adapter Kit		
01		Power Supply Programmer		
01		Dual Unit Programmable Power Supply 0 - 25 V 0 to -25 V at 2 A.		
01		High Current Programmable Power Supply 0 - 20 V @ 10 A		
01		Fastrace Probe		
01		Repair Ticket Printer		
01		HP-IB Instrument Interface		
01		91073A Prom Set for Micro-instruction Storage		
01		Test Fixture		
01		Self Test Adapters		
07		Volumes of Hardware and Software documentation		
01		On-Site installation by Hewlett-Packard Service		
02		92770A Digital Test Programming Course at Loveland Division		
18	Opt. 010	Programmable Driver/Comparator Card for 15 UUT Pins	1,100.00	19,800.00
02	Opt. 016	Logic Level Reference Card	875.00	1,750.00
01	Opt. 015	DTU Extender - Adds 12 Additional Driver/Comparator slots.	2,800.00	2,800.00
01	Opt. 005	Programmable Rate Generator	600.00	600.00
01	Opt. S08	Programmable Power Supply (HP 6266B 0-40 V at 5 A.	1,600.00	1,600.00
01	Opt. S06	Programmable Power Supply (6263B) 0-25 V at 2 A.	1,600.00	1,600.00
01	5022A	Digital Troubleshooting Kit	735.00	735.00
02	Opt. M32	9571 Maintenance Training (1 week)	750.00	1,500.00
01	Opt. XXX	Deletes 6227B Power Supply 0-20 V at 10 A	-1,600.00	-1,600.00

HUGHES AIRCRAFT COMPANY

Budgetary Quotation

QTY.	DESCRIPTION	PRICE
	HP 1000 Model 40, Consisting of:	
1	2176A Computer System which includes	$ 37,750
	1 ea., 2113A Computer with 128K Byte Standard Memory	
	1 ea., 7906/020 19.6M Byte Master Disc Drive and Interface.	
	1 ea., 29402B/200 Cabinet with Front Door	
	1 ea., 2645 Terminal with Interface	
	1 ea., 92067A/031 RTE-IV Operating System on Disc Cartridge	
	1 ea., Diagnostics Package on Mini-tape Cartridge	
	1 ea., System Hardware and Software Manuals	
	Also includes:	
	Factory Integration and Test On-Site installation Site Preparation Consultation Three Months On-Site Support	
	1 ea., Option 014, which deletes the Standard 128K Byte Memory	-4,500
1	HP 12788B Memory - 256K Byte High Performance Package	7,500
1	HP 2608A Line Printer with Option 210 which includes Interface and Documentation for use with HP 1000 System, 400 LPM	9,250 650

OPTIONAL ITEMS

1	HP 92063A + 020 IMAGE/1000 Data Base Management System	$ 2,500

HUGHES AIRCRAFT COMPANY

Budgetary Quotation (Cont.)

QTY.	DESCRIPTION	PRICE
1	HP 2621A CRT Terminal	$ 1,450
1	HP 12966A Terminal Interface	600
2	HP 22977A IMAGE/1000 DBMS Training (Five Days)	1,000
2	HP 22951B Introduction to HP Minicomputers	600
2	HP 22991A HP 1000 Disc Based RTE System Course (Ten Days)	2,000
3	HP 22976B S.E. Consultant (Three Days)	1,500

HEWLETT-PACKARD EXCEPTIONS TAKEN TO
HUGHES' DIGITAL PRINTED CIRCUIT BOARD TEST SYSTEM

SPECIFICATION DATED: May 21, 1979

---

1) 3.2.1.2.1.2.1 - The HP 7906A 20.M Byte Disc Drive that we have recommended includes both a removeable cartridge (10 MBytes), and a fixed NON-removeable disc. This allows the user to copy from one surface to the other and back the system up. We do make smaller drives if required; however, with data base management we recommend the 20.M Byte 7906A.

2) 3.2.1.2.1.4 - The HP 2608A Line Printer is a 400.LPM Printer. We recommend this for report generation using data base management.

3) 3.2.1.2.2.4 - The HP Programmable Rate Generator (Option 005) provides 5 MHz (±0.1%) signals at TTL levels. Many of our customers use a simple level translator circuit mounted on the test fixture to drive other logic families. Another solution is simply to purchase an HP-IB (IEEE 488) pulse generator or function generator/synthesizer.

4) 3.2.1.2.3.2 - We provide everything but the footswitch. There is a BNC jack on the front panel that is connected to a hand actuated switch. All that would be necessary is buying a footswitch and putting a BNC connector on the end of the cable.

5) 3.2.1.2.4.1. - The standard system contains an HP 6263A Power Supply which meets the need for your power supply Number 2. I have configured in a second 6263A for power supply Number 1. It has a 10 amp limit which is 2 amps too low. The reason 10 amp supplies are configured in is that the PC traces on our test fixture have a 10 amp limit. We can put, and have put in very heavy current supplies (50. Amps +); however, you will need to use a heavy wire rather than the PC Board test fixture trace to deliver the power. The 6263A has 10 MV resolution instead of 5 MV also.

The other supplies meet or exceed your requirements.

6) 3.2.1.7 - Installation and system performance testing is provided by Hewlett-Packard. The acceptance test criteria is defined as our 9571A System Performance Test and 9571A System Functional Test. I have attached listings of these tests from our service manual.

SECTION IIIE
TESTER COMPOSITE SCORES

- Table 1.0 – Total Scores
- Table 2.0 – Maintenance and Support Scores
- Table 3.0 – Test System Hardware Scores
- Table 4.0 – Test Programming Scores
- Table 5.0 – Tester Software Scores

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Rev. Jan. 1971 Vendor's Name _____

TABLE 1.0 - TOTAL SCORES

Factor	Gen Rad	Computer Automation	Hewlett Packard	Teradyne
I. Without Bias				
1.0 Matchup Report	95	97	81	95
2.0 Maintenance & Support	48	40	45	46.5
3.0 Test System Hardware	58.5	57	48	68.5
4.0 Test Programming	65	64	53	61
5.0 Tester Software	32.5	39	46	30
	299	297	273	301
II. With Bias				
1.0 Matchup Report	190	194	162	190
2.0 Maintenance & Support	91.2	76	85.5	88.35
3.0 Test System Hardware	117	114	96	137
4.0 Test Programming	234	230.4	190.8	219.6
5.0 Tester Software	185.25	222.3	262.2	171
	817.45	836.7	796.5	805.95
Divided by 1197 =	68.29%	69.89%	66.54%	67.33%

Note: See Tables 2.0 through 5.0 for score breakdowns.

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Rev. Jan. 1971 Vendor's Name _____

TABLE 2.0 – MAINTENANCE AND SUPPORT SCORES

	Characteristic	Gen Rad	Computer Automation	Hewlett Packard	Teradyne
1.	Size of Manufacturer	>100M 4 (4)	80M 3 (3)	>100M 4 (4)	>100M 4 (4)
2.	ATE Market Value of Manufacturer	54M 3 (3)	13M 2 (2)	>100M 4 (4)	>100M 4 (4)
3.	Number of ATE users of Manufacturer board test system (any type)	100 4 (4)	200-300 4 (4)	100 4 (4)	30-100 3 (3)
4.	Number static board testers sold of the same type	200 4 (4)	300 4 (4)	100 4 (4)	20-50 3 (3)
5.	Service Support of Manufacturer	excellent 4 (10)	good 3 (7.5)	excellent 4 (10)	good 3 (7.5)
6.	Warranty	90 days + 1 year 2 (3)	1 year 3 (4.5)	3 months 1 (1.5)	10 years 4 (6)
7.	MTBF	120 days 2 (4)	800 hrs. 1 (2)	850 hrs 1 (2)	2-3 months 1 (2)
8.	Support Equipment required	10K or less 4 (4)	10K or less 4 (4)	10K or less 4 (4)	10K or less 4 (4)
9.	Tester Self test Features	Semi Auto Fault Isol 3.5 (3.5)	Auto, Fault Isolation 4 (4)	Semi Auto Fault Isol 3.5 (3.5)	Auto Fault Isolation 4 (4)
10.	Design Philosophy of Tester	Commercial 1 (.5)	Commercial 1 (.5)	Commercial 1 (.5)	Commercial Ruggedized 2 (1)
11.	Test System Layout/ User Interface	Fair 2 (3)	Good 3 (4.5)	Good 3 (4.5)	Excellent 4 (6)
12.	Procured Logistic Elements	7 2 (2)	Not answered 0 (0)	4 2 (2)	1 1 (1)
13.	Government Agencies Procured Tester	8-12 3 (3)	Not answered 0 (0)	3 1 (1)	1 1 (1)
	( ) = Score times bias factor	(48)	(40)	(45)	(46.5)

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Information Media Department Standard MODULAR Keyline NOTE: LEFT HAND PAGE ONLY	Proof	Ink	Art	CRC	Log No. 99231 kn Vol. No.

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TABLE 3.0 – TEST SYSTEM HARDWARE SCORES

Characteristic	Gen Rad	Computer Automation	Hewlett Packard	Teradyne
1. Number of driver/ sensors	480 3 (4.5)	383 3 (4.5)	360 3 (4.5)	456 3 (4.5)
2. I/O pins switched to input/output via test program	yes 1 (6)	yes 1 (6)	no 0 (0)	yes 1 (6)
3. Pattern depth of one program load	Unlimited except disk limit 4 (6)	4,000 3 (4.5)	4,095 3 (4.5) more than	>4,095 4 (6)
4. Programmability of driver/sensors	2 families programmable 3 (4.5)	2 families programmable 3 (4.5)	2 families programmable ± 15 4 (6)	2 families programmable 3 (4.5)
5. Dynamic	No 0 (0)	No 0 (0)	No 0 (0)	yes 1 (5)
6. Go/No Go Test Method	Stored Patterns 3 (6.0)	Stored Patterns 3 (6.0)	Stored Patterns 3 (6)	Stored Patterns w/sig. anal. 4 (8)
7. Go/No Go throughput (@ 10,000 patterns)	10 sec 2 (4.0)	5-10 sec. 2 (4)	1-5 sec 3 (6)	Limited to 4,000: 25 sec 2 (4.0)
8. Diag Clip	2 clips up to 24 3 (3.0)	1 clip with pulse catching 6 (6.0)	None 0 (0)	None 0 (0)
9. Single Pin Probe	Yes, Smart, Pulse Catching 4 (8.0)	Yes, Smart, Pulse Catching 4 (8.0)	Yes, Smart, Pulse 4 (8)	Yes, Pulse Catching, State Sensitive, smart 5 (10)
10. Pin Isolation	Yes 1 (6.0)	No 0 (0)	No 0 (0)	Yes/electronic knife 1 (6.0)
11. IEEE Bus	Yes 1 (3.0)	Yes 1 (3.0)	Yes 1 (3.0)	Yes 1 (3.0)
12. Growth Potential	CPU, Hybrid 3 (4.5)	Dynamic, Hybrid, CPU 5 (7.5)	Mult.Prog.Stat CPU, Hybrid 4 (6)	Dynamic Hybrid, CPU 5 (7.5)
13. Test Fixturing	Good 3 (3.0)	Good 3 (3.0)	Excellent 4 (4)	Excellent 4 (4)
( )= Score time Bias factor	(58.5)	(57)	(48)	(68.5)

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TABLE 4.0 – TEST PROGRAMMING SCORES

Characteristic	Gen Rad	Computer Automation	Hewlett Packard	Teradyne
1. IC Modeling	8 (12)	7 (10.5)	4 (6)	4 (6)
2. Standard LSI Library	80 8 (8)	80 8 (8)	None 0 (0)	10-20 4 (4)
3. Circuit Complexity	7 (7)	7 (7)	7 (7)	6 (6)
4. Circuit Mod. Convenience	10 (5)	9 (4.5)	8 (4)	8 (4)
5. Good Circuit Sim.	5 (5)	5 (5)	5 (5)	6 (6)
6. Fault Simulation	7 (7)	9 (9)	6 (6)	9 (9)
7. ATG Feature	1 (1)	0 (0)	8 (8)	9 (9)
8. Test Language	macro, high level 5 (5)	macro, high level 5 (5)	High level 2 (2)	high level 2 (2)
9. Manual Programming	15 (15)	15 (15)	15 (15)	15 (15)
( ) = Score times bias factor	(65)	(64)	(53)	(61)

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Rev. Jan. 1971 Vendor's Name _____

TABLE 5.0 – TESTER SOFTWARE SCORES

Characteristic	Gen Rad	Computer Automation	Hewlett Packard	Teradyne
1. Operating System	Gen. Purpose 3 (3)	Gen. Purpose by Mfg. 4 (4)	Gen. Purpose by Mfg. 4 (4)	Special Purpose 2 (2)
2. Background/ Foreground	Prog. & Test 6 (12)	Prog. & Test 6 (12)	Prog. & Test w/time share 10 (20)	Test only w/outside time share 4 (8)
3. Translators, Converters Tester Output Avail.	GR 2225 output 1 (.5)	4 trans. w/D4-LASAR 6 (3)	None 0 (0)	D4-LASAR, two-post processors 6 (3)
4. Data Logging	Record only 1 (5)	Record and Analysis 2 (10)	Record and Analysis 2 (10)	Record only 1 (5)
5. On line user aids/ controls	Good 3 (12)	Excellent 4 (16)	Good 3 (12)	Good 3 (12)
( ) = Score times bias factor	(32.5)	(39)	(46)	(30)

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Information Media Department Standard MODULAR Keyline NOTE: RIGHT HAND PAGE ONLY	Proof	Ink	Art	CRC	Log No. ~~99123~~ 99231 Vol. No. km

Rev. Jan. 1971 Vendor's Name _____

SECTION III F
TEST SYSTEM MEASURED PERFORMANCE

NOTE: This section is comprised of a system performance test report.

SYSTEM PERFORMANCE TEST REPORT

FINDINGS AND RESULTS

by

Dr. L. P. Henckels

CONTENTS

Benchmark Test Results ..... III. F-0
Introduction ..... III. F-1
Description of Test Case ..... III. F-1
Performance Scores ..... III. F-6
Conclusion ..... III. F-9

BENCHMARK TEST RESULTS

Each test system was evaluated with a benchmark circuit board which was specifically developed for this analysis.

The highest performance score was achieved on Teradyne's system, consisting of a Digital Equipment VAX CPU System for test programming using LASAR and the Teradyne L135 Tester. Among the three remaining minicomputer-based test systems, GenRad's 1795HD System achieved the best score.

A small benchmark test case was developed to evaluate the performance of the four candidate testsystems. The test case was programmed and then tested on each test system. The performance of each system was measured both during programming and during failure diagnosis.

Introduction

The selection criteria of the final test system so far was strictly based on data received from vendors and a Selection Guide for Digital Test Program Generation Systems (Ref. 1). However, the performance of any one system is greatly impacted by its implementation quality which was evaluated with a benchmark test case as described below.

To program a 50 IC test case typically requires 200 man hours (see section 2, subsection F). Thus, it was not possible to run such a large test case on each system because of constraints in both time and costs. Instead, a small, specially designed benchmark test case was developed which could test out the performance of each system.

Description of Test Case

The purpose of the test case is to evaluate the performance of each test system, namely its accuracy, throughput, and overall ease of use. To measure these performances, two small circuits were developed:

Test Case 1 - DPRØX Circuit

This 5 IC test case was carefully designed to test all aspects of the system. The circuit consisted of two 5101 CMOS RAMS (see Figure 1) which are uncommon and which, therefore, had to be modeled. The address lines of the RAMS were fed by a TTL 74161 counter which was initialized via a power-up RC network. All data to and from the RAMS, which were wired-or

Ref. 1 Henckels, Haas and Brown, "Selection Guide for Digital Test Program Generation Systems", HHB, Inc., Upper Saddle River, NJ, 07458, 1978.

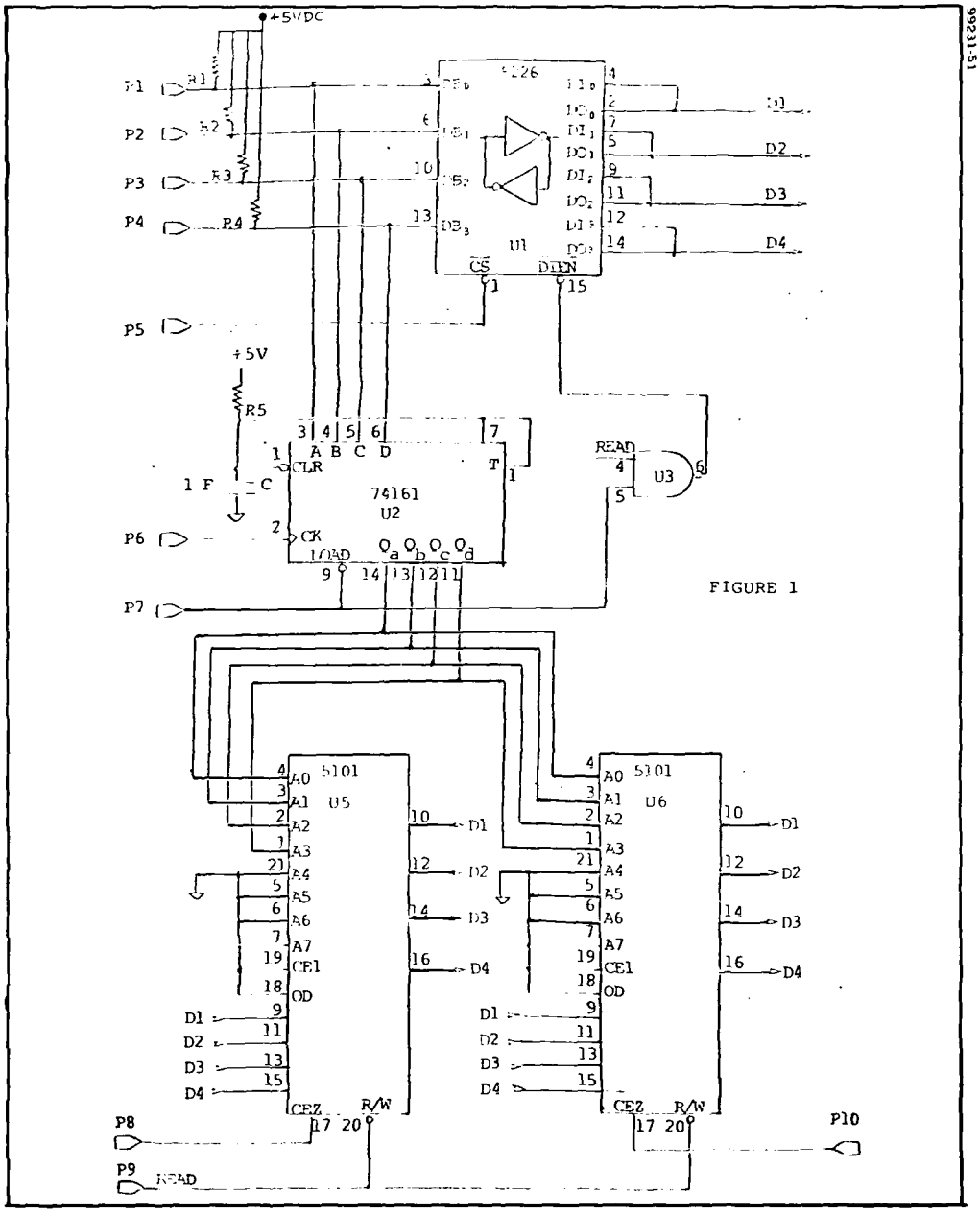

+5VDC
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
R1
R2
R3
R4
R5
1 F
U1
U2
U3
U5
U6
74161
5101
CLR
CK
LOAD
CS
DIEN
READ
CE1
CE2
R/W
OD
D1
D2
D3
D4

FIGURE 1

in parallel, were channeled through a bidirectional transceiver (8226).

This mixture of TTL and CMOS logic was chosen to evaluate the testers capability of handling several logic families. (Multiple threshold levels, low current pin isolation capability). The 8226 transceiver was selected to evaluate the system capability of handling bidirectional, tristate busses both on the IC level as well as on the board level. The 74161 was programmed into illegal states to observe the systems capability to flag such conditions. The power-up reset circuit, the pullup resistors and the ground pins were included to demonstrate how easily the system can handle such special circuits. Overall the circuit was designed to contain bus structures and feedback loops which are typical in today's logic but are more difficult to test.

Test Case 2 - DPRØ2 Circuit

This 11 IC circuit (see Figure 2) was developed to measure simulation accuracy. As such, it is a mathematical or hypothetical case and no physical board was built for it. The accuracy measurement included asynchronous pulses, logic delay characteristics, oscillations, $X\overline{X}$ cancellation, X detection, etc. In particular, the following circuits had been included:

- U1 will generate a pulse (asynchronous reset).
- U2 cannot be initialized.
- U6 Pin 3 is always one due to X and $\overline{X}$ cancellation.
- U9 is 6.6 milliseconds.
- U7 latch will be tested for oscillation.

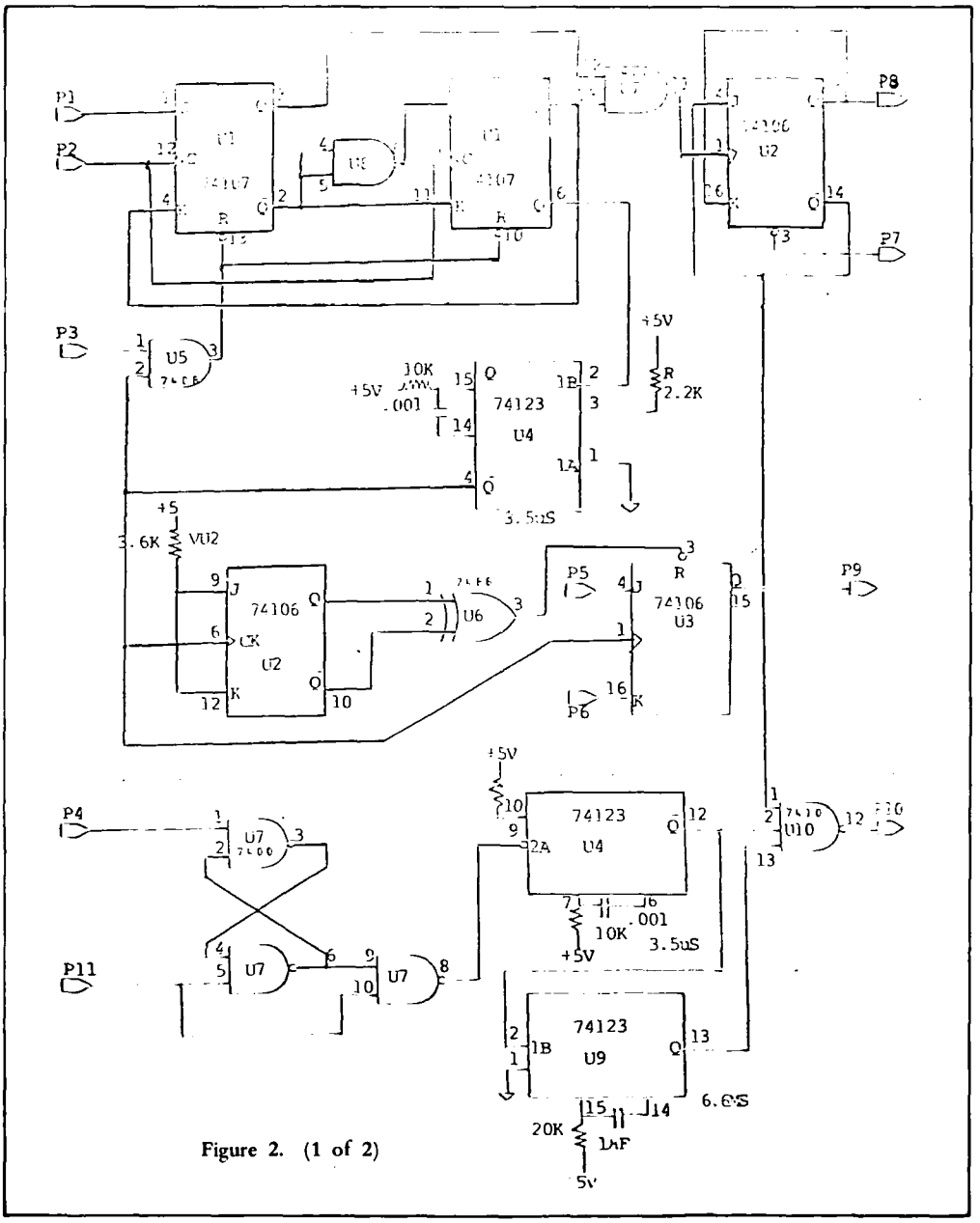


Figure 2. (1 of 2)

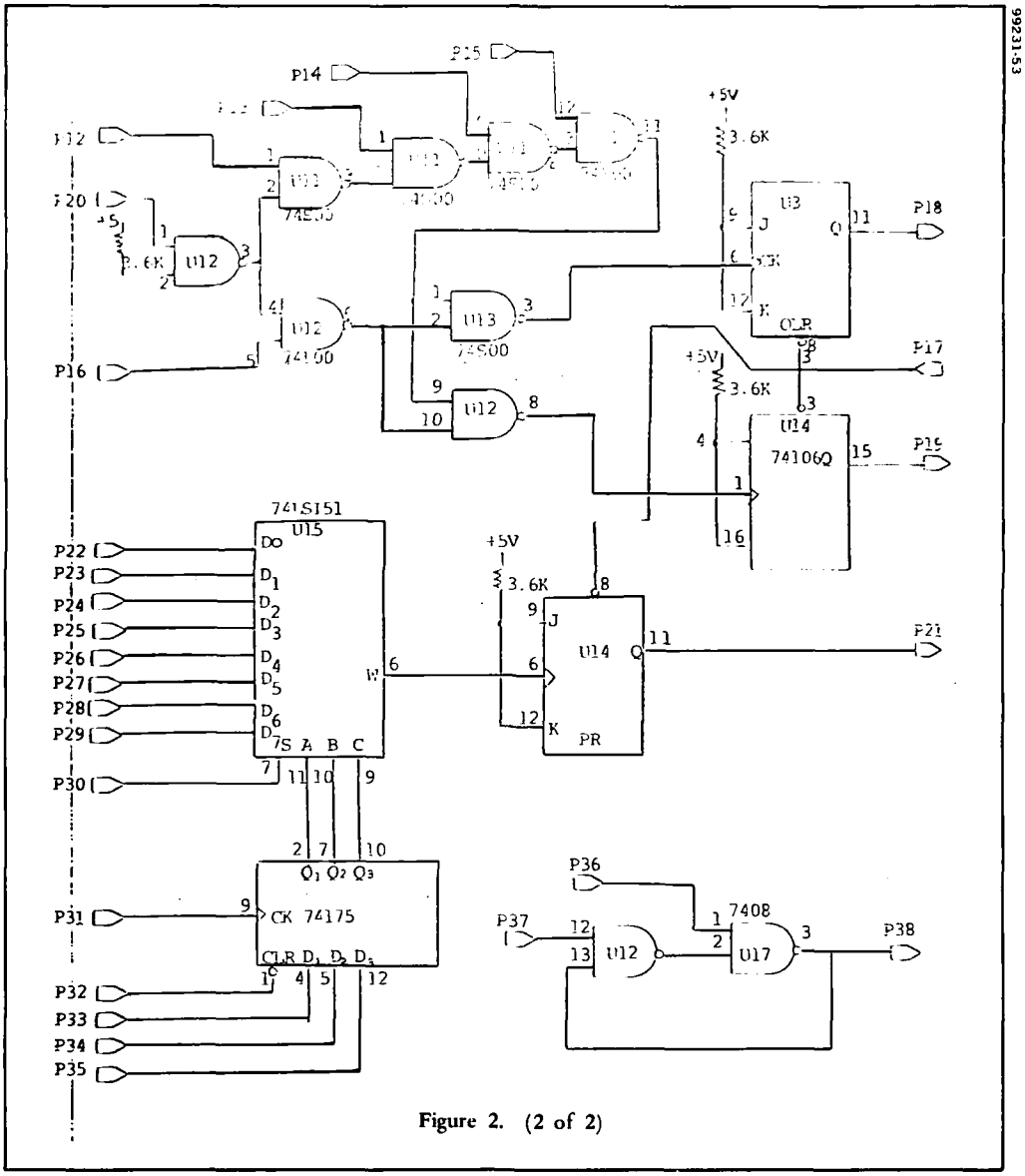


Figure 2. (2 of 2)

. U11 and U12 converge at U13 and cause a pulse. The four cascaded 74SØØ gates have a total delay of 12 nanoseconds, the 74LØØ gate has a delay of 35 nanoseconds.

. The U15 decoder will generate a pulse if the data lines are high during control line changes.

. P37 stuck-at-one will cause an oscillation.

Performance Scores

Final performance scores were based on the first test case, (DPRØX Board) only. This 5 IC board proved to be much more difficult to test than anticipated and as a result, the time at each manufacturers site was insufficient to adequately work with the second test case.

Simulation Criteria

. Simulation Accuracy (Ø to 12)

. Fault Simulation Time (Ø to 12)

. Ease of Use (Ø to 12)

Tester Criteria

. Accuracy of Diagnostics (Ø to 8)

. Probe Time (Ø to 8)

. Accuracy of Pin Diagnostics (Ø to 8)

System Criteria

. Overall Ease of Use (Ø to 12)

The simulation accuracy was based on an analysis of both the good circuit simulation data and the fault detection data. HP's TESTAID III System scored highest (see Fig. 3) in this category identifying properly when each

	MAXIMUM RATING	COMPUTER AUTOMATION	GENRAD	HP	TERADYNE
Simulation Score					
Accuracy	12	6 (9)	9	11	8 (11)
Time	12	9 (10)	9	6 (9)	12
Ease of Use (work around)	12	9	10	6 (9)	6 (9)
Testing Score					
Accuracy	8	1 (7)	6 (7)	3 (6)	8
Probe Time	8	3	2 (3)	4	8
Pin Diagnostics	8	2	6	Ø	6
System Score					
Ease of Use	12	9	11	9	8
TOTAL SCORE	72	39 (49)	53 (55)	39 (48)	56 (62)

99231-54

NOTES
1) SHADED SCORES WERE NOT USED IN THE FINAL TEST SYSTEMS SELECTION (SEE REPORT TOPIC 2.F-2)
2) ONLY THE RAW SCORES IN PARENTHESES AND NON-SHADED SCORES ARE USED IN THE SYSTEMS MEASURED ACHIEVEMENT SCORE IN TABLE II OF REPORT TOPIC 2.F-2

BENCHMARK TEST SCORES

Figure 3

fault was detected including X-detections (unknown states propagated to the edge connector due to a fault).

The fault simulation time was measured by simulating all stuck-at faults (node and pin level) at the IC pin level. Teradyne scored highest in this category with a normalized simulation time of roughly 14 milliseconds/fault. GenRad achieved the next highest score with a normalized simulation time of 15.9 milliseconds/fault.

The ease of use of the simulation system was based on the efforts involved in fault modeling, circuit modeling and the development of test programming, i.e., the development of the proper simulation data. GenRad scored highest in this category requiring the least IC modeling effort, the least work around in circuit modeling and providing the best interactive capabilities in preparing the simulation data.

The performance scores on the tester were derived by inserting five faults into the DPRØX Board. Teradyne scored highest in two out of three categories by accurately locating each fault in approximately one minute/fault. The capability to isolate a fault to the IC pin level rather than just the IC node level is only available by GenRad (DRM) Teradyne (Electronic Knife) and Computer Automation, which presently performs only shorts analysis. While Teradyne's Electronic Knife has higher sensitivity in isolating faults to the pin level, GenRad's DRM can identify shorts between any two IC pins. Thus, the overall accuracy of fault isolation beyond the node level was roughly the same on both Teradyne's and GenRad's systems.

The score for the overall ease of use on the system level was again highest for GenRad. The menu type system executive, their

screen editing capabilities and their combined simulation/test capabilities on one test system were major factors in deriving this score. However, the debug capabilities and aids available on the test system are strongest on the Computer Automation and Teradyne systems.

Conclusion

Based on these performance scores, Teradyne ranks highest with 56 points out of 72 followed closely by GenRad with 53 points (see Figure 3). For various reasons, the test case could have caused pessimistic test scores for each test system. Allowing for these uncertainties, we have enclosed in parenthesis our most optimistic scores. Again, Teradyne scored highest with 62 points followed by GenRad with 55 points.

It is worth noting that Teradyne's high score is in large part achieved because of its excellent probe and diagnostic system on the L135 test system. In particular, the average probe time on Teradyne's system for all 5 faults inserted was approximately 1 minute/fault. In comparison, the average probe time on GenRad's system was 5 minutes. Similarly, Teradyne scored highest in accuracy by isolating all 5 faults down to the node level and even further down to the pin level using the high impedance measurement of the electronic knife. Finally, their interactive probe displays for debugging are truly superb to any other system evaluated.

While Teradyne scored highest on the tester, GenRad scored highest on test programming (simulator) and overall ease of use. For example, the user interface of GenRad's CAPS System with its menu type executive and screen editor is simple and efficient to use. None of the other systems have this setup and require, therefore,

higher skills from the user.

Another example is IC modeling. When modeling the 5101 chip, a rather complex gate level model was developed by Teradyne. At HP the user had to worry about the insertion of delays which took two trial runs before we got it right. Furthermore, in modeling the 8226 chip, pseudo pins had to be set up at both Teradyne and HP in order to handle the bidirectional bus pins. Again, these are added complexities far in excess of what is required for the GenRad system. In circuit modeling for HP or Teradyne, the user had to worry about input and output pins as well as label each node in order to process the circuit. In comparison, this task is often performed by clerical people on GenRad systems who are unfamiliar with digital logic.

Finally, the interactive display capabilities and the flexibility in selecting faults for simulation are unmatched by any of three other vendors. We feel that this overall ease of use, combined with its integrated tester interface (including the capability to resimulate and reprocess on the test system itself) is unmatched by the other systems.

INTERIM REPORT ATT IV – MM&T – DFI FOR PCBs – TESTABILITY INVESTIGATION

TESTABILITY INVESTIGATION –

ATTACHMENT IV TO INTERIM REPORT (BASIC EFFORT)

MANUFACTURING METHODS AND TECHNOLOGY FOR 'DIGITAL FAULT ISOLATION FOR PRINTED CIRCUIT BOARDS'

PROJECT NO. R783242

CONTRACT DAAK40-78-C-0290
25 AUGUST 1979
CDRL A003

TESTABILITY INVESTIGATION –
ATTACHMENT IV
TO INTERIM REPORT (BASIC EFFORT)

Manufacturing Methods and Technology for
'Digital Fault Isolation for Printed Circuit Boards'
Project No. R783242

Prepared for
U.S. Army Missile Research and Development Command
Redstone Arsenal, Alabama 35809

Project Officer: G. Little
DRDMI-EAT
(205)-876-3848

Contract No. DAAK 40-78-C-0290
CDRL A003

Prepared by

Hughes Aircraft Company
Ground Systems Group
Fullerton, California 92634

Report Date: 25 August 1979
FR79-12-669

FOREWORD

This report presents the recommendations and conclusions with supporting data resulting from the Basic Effort phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology that will enable detection, identification, and location of digital faults in advanced digital missile electronic systems. Emphasis is placed on the fault diagnosis of large printed circuit boards containing complex digital hybrid microelectronic circuits to be used in the 1980's. The identified technology provides the capability to isolate digital faults to the minimum size component level, using state-of-the-art automatic test equipment.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the development of digital fault isolation methodology, and the identification of the corresponding optimum available automatic test hardware.

The subsequent contract option phase of this project involves the purchase, setup, and demonstration of the selected fault isolation hardware/software system, using the developed techniques.

CONTENTS

SECTION IVA – OVERVIEW AND SPECIFICATION EVALUATION SUBTASK

1.0 Scope 1
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SECTION IVA
OVERVIEW AND SPECIFICATION EVALUATION SUBTASK

TESTABILITY INVESTIGATION

1.0 Scope

1.1 Purpose - The purpose of the Digital Fault Isolation Testability study is to determine digital PCB testability methods for existing, new design, and benchmark PCBs, and to evaluate testability standards in military specifications.

1.2 Scope of the Effort - The task was divided into a preliminary survey phase and a detailed study phase. The preliminary survey consisted of two parts: first, a survey of military specifications, standards, and handbooks to select those having testability related factors. The second preliminary part was a survey of the literature to select documents specifically related to digital PCB testability, but in a broad sense of the term. Both surveys were conducted keeping in mind the goal of digital testability for the 1980s.

The study phase was three-pronged. The first consisted of a detailed examination of the selected military specification documents, details of which are contained in paragraph 3.0 Subtask: Evaluate Military Specifications (para 3.0 thru 3.4.4) and Appendix I, consisting of exhibits associated with paragraph 3.0. The main result is a recommendation for three documents, a testability standard, a test program sets standard, and a testability handbook. Specific suggestions regarding incorporation of existing documents into those recommended are included. The study also contains suggestions for updating existing specifications documents to reflect the digital testability needs of the 1980s.

The second part of the study phase is a testability design guide for digital PCBs for the 1980s, a unique consolidation and summarization of significant rules, practices, suggestions and studies pertinent to the testability of digital PCBs. Details of this study are contained in para 4.0 Subtask: Testability Design Guide for Digital PCBs (para 4.0 thru 4.3.9.15).

The third part of the study is a set of specific recommendations for improvement of MIRADCOM benchmark PCB cards. Details of these recommendations are contained in para. 5.0 Subtask: Testability Improvement of Benchmark PC Cards (para 5.0 thru 5.3.3.4).

2.0 References - Specific document references are contained in the individual studies. 3.0 Subtask: Evaluate Military Specifications, contains in effect a bibliography of military specifications on testability. 4.0 Subtask: Testability Design Guide, contains an extensive bibliography on testability documents (para 4.3.9 thru 4.3.9.15).

3.0 Subtask: Evaluate Military Specifications

3.1 General Considerations

3.1.1 Purpose - The purpose of this subtask is to review existing military specifications with respect to their applicability to testability standards to meet the digital electronic technology requirements of the 1980's. Since a need was determined to exist, specific recommendations are made for military specifications pertaining to testability requirements applicable to 1980's technology.

Types of documents reviewed were military specifications, military standards and military handbooks.

3.1.2 Follow-on Tasks - Proposed or contemplated specifications documents which should be incorporated into this survey, but which are not available for inclusion in the study are: (1) proposed MIL-STD-2084, the replacement for AR-10A, (2) MIL-STD-proposed (AS) referenced in MIL-STD-2076(AS) (this may be MIL-STD-2084 (proposed)), (3) standards that may emanate as results of the Sperry and Westinghouse MATE studies for the Air Force (expected completion early 1980), (4) MIL-STD-1326A in process of being revised.

3.1.3 Precedence of Information - Significant references are made to military specifications and paraphrasing and elision are used freely. In case of conflict between this document and a referenced specification, the specification governs.

3.2 Format of the Evaluation Report

3.2.1 Division into Groups - The military specifications evaluated in this report are divided into two groups as follows: (1) specifications that pertain to testability characteristics, (2) other documents considered.

3.2.2 Subdivisions of Group 1 - Group 1 has been further divided into five subgroups. Group 1.1 contains specifications with numerous references to testability related factors. Group 1.2 contains those with a moderate number of references to testability characteristics. Group 1.3 encompasses specifications with slight references to testability characteristics. Group 1.4 are those specifications with minor or indirect references to testability characteristics. The relationship of Group 1.5 specifications to testability is solely through pertinent or associated definitions.

3.2.3 Contents of Report for Subgroups of Group 1 - For subgroups 1.1 through 1.5 the contents of each document are summarized, and, where applicable, a recommendation is made for improving the document for testability. In the majority of cases the comments are supported by an exhibit in Appendix I consisting of more detailed analysis and/or specific quotations from the referenced specification. The documents of Group 1 form a bibliography of testability related military specifications.

3.3 Recommendations

3.3.1 Summary

- This survey has pointed up the need for several military documents pertaining to testability. It is recommended that three such documents be considered; either as revisions of existing documents or new documents as appropriate. Details are in paragraph 3.3.2.

  1. A military standard on testability
  2. A military standard on test program sets
  3. A military handbook on testability design, prediction, and measurement techniques.

- It is also recommended that certain existing specifications documents be reviewed and updated to incorporate testability related recommendations. Details are in Paragraph 3.3.3 and Appendix I.

3.3.2 Recommendations for New Documents

3.3.2.1 Basis for Contents of New Documents - The recommendations of this survey of military specifications and the results of the associated survey of testability techniques Paragraph 4.0 provide a basis for establishing the contents of these three documents. Application of the specifications to the recommended documents is outlined in the matrix in Paragraph 3.3.2.2. A generalized summary of the suggested substance for each of the documents follows the matrix.

3.3.2.2 Application Matrix of Existing Specifications to Proposed Documents

Existing Specification Document	Candidate for Consolidation into		
	Testability Standard	Test Program Sets Standard	Testability Handbook
AR-10A (NOTE 1)	Yes (NOTE 1)		
MIL-STD-415D	Yes		
MIL-STD-1326 (NAVY)	Yes		
MIL-STD-2076 (AS)	Yes		
MIL-STD-2077 (AS)		Yes	
MIL-E-11991D (MI)			Yes
MIL-M-24365A (SHIPS)	No	No	No
MIL-STD-1519 (USAF)		Yes	
MIL-HDBK-239 (NAVY)	No		Source
MIL-T-24309 (SHIPS)	Yes	Yes	
MIL-T-28800B	No		
MIL-STD-1378B	Source		

NOTE 1: AR-10A is to be replaced by MIL-STD-2084 (pending).

3.3.2.3 Action to be Taken on Existing Specifications - When testability elements are stripped from existing documents these documents should be amended, as applicable, to incorporate the removed testability functions by reference to the new testability documents. It is suggested that each of the recommended documents be sufficiently comprehensive to replace several current documents.

3.3.2.4 General Substance of Proposed Documents

3.3.2.4.1 Military Standard on Testability - This standard would establish definitions for testability, testability prediction, and testability measurement. For assemblies of complexity from WRA (weapons replaceable assembly) to sub-SRA (sub-shop replaceable assembly), it would establish testability design requirements and prediction and measurement standards and methods to ensure adequate test comprehensiveness to achieve the required diagnostic resolution.

It would also incorporate all applicable testability elements in existing specifications and standards. In addition it would establish management responsibility for enforcement of the standard and engineering responsibility for its application.

3.3.2.4.2 Military Standard on Test Program Sets - This document would be a companion to the standard on testability. Its objective is to establish all of the required elements needed to test a specific hardware unit, and to determine that these elements are performance ready. It includes consideration of the established maintenance concept for the system that uses the hardware units. It defines types of tests to be performed and the order of testing, including ATE self-test; and discusses design data requirements for the test programs. It describes means of implementing tests, test facilities requirements, and adapter design considerations. It also addresses utilization of the BIT/BITE concept in the test strategy. Furthermore it provides means of measuring the testability of a UUT (unit under test) to establish that the prediction established during the testability analysis is attained. This in turn establishes achievement of the required level of diagnostic resolution.

3.3.2.4.3 Military Handbook on Testability - This document would be a specific workbook of various testability design techniques, procedures for predicting testability, and methods of testability measurement. It would include means of establishing the test comprehensiveness needed to achieve a desired diagnostic resolution for a UUT, and methods for measuring that resultant diagnostic resolution. It would establish the means of implementing the requirements imposed by the military standard on testability. It would also describe alternate ways, where appropriate, of achieving requirements imposed by the military standard on test program sets.

3.3.3 Recommendations for Existing Documents

3.3.3.1 Specifications with Numerous Testability References - The following specifications contain numerous references to testability related factors:

3.3.3.1.1 AR10A *Naval Air Systems Command* 1 Jan 1969
Maintainability of Avionic Equipment and Systems, General

- Note: MIL-STD-2084 (pending will obsolete AR10A)

- Comment: This document contains significant testability criteria; it specifies the maintainability and built-in-test requirements for avionic equipment. The attached exhibit highlights significant paragraphs of the

specification that pertain to testability criteria, and also has definitions from the specification that apply to testability. (See Exhibit 3.3.3.1.1 in Appendix I.)

- Recommendation: Withhold recommendation until MIL-STD-2084 (pending) is available for review. It will probably provide the core for the recommended testability standard.

3.3.3.1.2 MIL-STD-415D Military Standard 1 Oct 1969
Test Provisions for Electronic Systems and Associated Equipment, Design Criteria for

- Comment: This standard relates directly to establishing testability criteria. It separates test provisions into four classes:
  - Class A - performance evaluation
  - Class B - malfunction isolation to a replaceable unit
  - Class C - malfunction isolation to a replaceable module or replaceable assembly.
  - Class D - test points (in the broad sense) to isolate malfunctions of a replaceable module or assembly to the individual piece part level.
- The standard contains pertinent definitions which apply to Automatic Test Equipment (ATE):
  - test provisions
  - test points
  - replaceable unit
  - replaceable module
- The contractor is required to analyze the design and determine test provisions necessary for operation and maintenance that are compatible with the approved maintenance concept. There are also specific provisions for test point marking that would be difficult to implement in the denser circuitry of the 1980's.

  Though the provisions of this standard are generally applicable to tomorrow's electronic systems, some of the terminology and requirements are obsolete. (No exhibit.)
- Recommendation: This document should be used as a substantial contributor to the recommended testability specification.

3.3.3.1.3 MIL-STD-1326 (NAVY) Military Standard 15 Jan 1968
Notice 1 1 Apr 1969
Test Points, Test Point Selection and Interface Requirements for Equipments Monitored by Shipboard On-Line Automatic Test Equipment

- Note: A draft revision of this standard, MIL-STD-1326A dated 27 Feb 1976, is referenced in the literature.(1)

- Comment: This document gives rules for optimum test point selection for mating with ATE, including interfacing guidelines and procedures for documenting the selection process. Significant terms are defined. Paragraphs 5 through 5.7.1 place restrictions on the ATE that may not be applicable in their entirety to the ATE and technology of the 1980's. (See exhibit 3.3.3.1.3 in Appendix I.)

- Recommendation: This document should be used as a significant contributor to the specification on testability. Retained portions should be updated to be applicable to the technology and testing requirements of the 1980's.

(1) R. D. SCHNEIDER, General Electric Co., Aircraft Equipment Div., Utica, N.Y., Standardization of Design Guides, Plans, Terms, and Definitions. Industry/Joint Services Automatic Test Conference & Workshop San Diego, CA., Apr 1978. pp. 126-128

3.3.3.1.4 MIL-STD-2076(AS) Military Standard 1 Mar 1978
Unit Under Test Compatibility with Automatic Test Equipment, General Requirements for

- Comment: This is a relatively new standard containing requirements for UUT/ATE compatibility, together with testability requirements for UUT's. It defines ATE compatibility, failure, and (by reference) replaceable assembly classifications. It specifies requirements for diagnostic fault isolation for the assembly classes, lists some compatibility design guides and test signal conditioning circuits, quantitatively matching UUT and ATE design and performing other necessary fault analysis tasks. (See exhibit 3.3.3.1.4 in Appendix I.)

- Recommendation: This document should be used as a significant contributor to the recommended testability standard.

3.3.3.1.5 MIL-STD-2077(AS) Military Standard 9 Mar 1978
Test Program Sets, General Requirements for

- Comment: This is a relatively new standard that classifies the types of tests to be performed on UUT's and gives the order of testing. It contains requirements for utilization of BIT/BITE, guidelines for designing the UUT/ATE interface device (adapter), adapter tests required, probe connection guidelines. It contains specifications for a diagnostic resolution table to correlate faults with probable cause. It also has a glossary of terms and a list of approved abbreviations. (See exhibit 3.3.3.1.5 in Appendix I.)

- Recommendation: This document should form the core of the recommended specification on test program sets.

3.3.3.2 Specifications with Moderate Testability References - The following specifications contain a moderate quantity of references to testability related factors.

3.3.3.2.1 MIL-E-11991D(MI) Military Specification 27 Feb 1976
Electronic, Electric, and Electro-mechanical Equipment, Guided Missile and Associated Weapons Systems, General Specifications for

- Comment: Specific references to testability criteria include accessibility to test points and terminals, built in test equipment, design of closed loop circuits for testability, definition of equipment failure, ease of adjustment and ease of maintenance. (See exhibit 3.3.3.2.1 in Appendix I.)

- Recommendations: This document should be used as a contributor to the recommended testability handbook. Incorporate in it elements of testability and test prediction by reference to MIL-STD-(testability) (to be written).

3.3.3.2.2 MIL-M-24365A (SHIPS) Military Specification 20 Jul 1970
Maintenance Engineering Analysis: Establishment of and Procedures and Formats for Associated Documentation; General Specifications for

- Comment: This specification relates specifically to maintenance engineering analysis and only indirectly to testability. There is considerable reference to testability criteria and other closely related elements. An extract of applicable paragraphs is appended. (See exhibit 3.3.3.2.2 in Appendix I.)

- Recommendation: Incorporate definitions for testability and test prediction by reference to MIL-STD-(testability) (to be written). Incorporate the application of testability prediction into Worksheet III.

3.3.3.2.3 MIL-STD-1519 (USAF) Military Standard 17 Sep 1971
Notice 1 1 Aug 1977
Test Requirements Document, Preparation of

- Comment: This specification has considerable information pertaining to test point location, test point connectors, test point data requirements. It also has guidelines governing specific means of test implementation. An extract from applicable paragraphs is appended. (See exhibit 3.3.3.2.3 in Appendix I.)

- Recommendation: Incorporate definitions for testability, testability prediction, and measurement by reference to MIL-STD-(testability) (to be written). This document should be used as a contributor to the recommended specification on test program sets.

3.3.3.2.4 MIL-HDBK-239(NAVY) Military Standardization Handbook 5 Sep 1973
Notice 1 20 Aug 1976
Navy Standard Electronic Module Program Application Handbook

- Comment: Though this document is oriented specifically to the Navy Standard Electronic Module Program, parts of it can, with minor modification, be adapted to other module designs. Other parts can, by the principle of logical extension, direct good design practices to other types of module development efforts. Specific areas of similarity are noted in the exhibit. (See exhibit 3.3.3.2.4 in Appendix I.)

- Recommendation: This document should be used as a significant source for the recommended testability handbook. Modifications to the specifications are not recommended because of the unique function it serves.

3.3.3.3 Specifications with Slight Testability References - The following specifications contain slight references to testability related factors.

3.3.3.3.1 MIL-T-24309 (SHIPS) Military Specification 1 Sep 1967
Amend 1 (Superseded by Amend 2)
Amend 2 29 Dec 1967
Technical Support Plan for Electronic Equipment

- Comment: This specification pertains to general maintenance requirements for (modular) electronic equipment. It contains a moderate amount of information that pertains to testability. Included are the maintenance concept, maintenance plan, test point data, sample maintenance document formats, schematic requirement to show test points, test and test facilities data. (See exhibit 3.3.3.3.1 in Appendix I.)

- Recommendation: Incorporate the definition for testability and definitions and requirements for testability prediction and measurement by reference to MIL-STD-(testability) (to be written). This document should be used as a contributor to the recommended specifications on testability and test requirement sets.

3.3.3.3.2 MIL-T-28800B Military Specification 9 Feb 1976
Amend 1 20 Jul 1977
Test Equipment for Use With Electrical and Electronic Equipment, General Specification for

- Comment: This specification indirectly relates to testability through the requirements placed on test equipment, including automatic test equipment (ATE). It specifies three types of test equipment:

  - Type I - Military
  - Type II - Commercial that meets some military requirements
  - Type III - Commercial that meets specific MIL-T-28800B requirements.

- It also subcategorizes test equipment into seven (7) classes according to intended location and use. Criteria related to testability include BIT

(built-in-test) and self-test capability; test point selection, accessibility, and identification; built-in adjustments; maintainability requirements, fault isolation and localization capabilities; interchangeability of parts; ease of installation; and ease of maintenance. (See exhibit 3.3.3.3.2 in Appendix I.)

- Recommendations: Incorporate testability design guides, and testability prediction and measurement requirements by reference to MIL-STD-(testability) (to be written). Incorporate requirements for testing and test requirements by reference to MIL-STD-(test requirement sets) (to be written) so the test equipment itself will be easy to test.

3.3.3.3.3 MIL-STD-1378B Military Standard 21 Dec 1977
Requirement for Employing Standard Electronic Modules

- Comment: This document contains specific requirements for testing digital SEM's including both parametric and functional type testing. By extension these requirements can be applied to other types of digital modules. Selected paragraphs concerning functional testing have been so modified and are referenced in the exhibit. (See exhibit 3.3.3.3.3 in Appendix I.)

- Recommendation: This document should be used as a source for the recommended testability specification. Modifications to it are not recommended because of the unique function it serves.

3.3.3.4 Specifications with Minor or Indirect Testability References - The following specifications contain minor or indirect references to testability related factors.

3.3.3.4.1 DOD-E-8983C Military Specification 29 Dec 1977
Electronic Equipment, Aerospace, Extended Space Environment, General Specification for

- Comment: The following paragraph excerpts from DOD-E-8983C pertain to testability related factors. (See exhibit 3.3.3.4.1 in Appendix I.)

  - 3.4.2 Detailed Mechanical and Electrical Design ***(The portion that pertains to isolation of redundant item failure propagation) ***

  - 3.8.3 Maintainability (The requirement for no scheduled maintenance or repair.) ***

  - 3.8.4 Durability (The requirement for control of degredation in performance.) ***

- Recommendation: For application to manufacturing testing only, incorporate testability criteria, and testability prediction and measurement by reference to MIL-STD-(testability) (to be written).

3.3.3.4.2 MIL-STD-454F Military Standard 15 Mar 1978
Notice 1 1 Sep 1978
Standard General Requirements for Electronic Equipment

- Comment: The following requirements pertain to testability related factors. (See exhibit 3.3.3.4.2 in Appendix I.)
  - Requirement 32 Test Provisions
  - Requirement 36 Accessibility
  - Requirement 72 Substitutability
- Recommendation: Requirement 72 should be amended to provide the additional requirement that substitution of parts shall not degrade the testability characteristics of the next higher assembly.

3.3.3.4.3 MIL-STD-470 Military Standard 21 Mar 1966
Maintainability Program Requirements (for Systems and Equipments)

- Comment: Testability is a sub-discipline of maintainability; it provides means whereby a critical and time-consuming part of the maintenance task can be significantly expedited. However in this document there are no significant references to testability, its prediction, or its measurement. (No exhibit.)
- Recommendation: Incorporate into this specification testability prediction as a part of the maintainability analysis.
- Specific recommendations pertinent to particular paragraphs of MIL-STD-470 are listed below:
  - 3. DEFINITIONS

    (Add definitions for testability, testability prediction, and testability measurement by reference to MIL-STD-(testability) (to be written).
  - 5.4 Establish Maintainability Design Criteria

    a. Reduce the complexity of maintenance by *** (Add between (2) and (3):

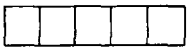
    "Providing adequate testability through incorporation of design features specifically added to enhance test capabilities as specified in MIL-STD-(testability) (to be written). The maintainability analysis will include an analysis of testability as specified in para. (tbd) of MIL-STD-(testability) (to be written). The calculated testability prediction shall be included in the maintainability analysis, and shall not be less than the value established by (the contracting documents)."
  - 5.11 (Include provisions for testability measurement in the Maintainability Demonstration Plan and the Maintainability Demonstration).

3.3.3.4.4 MIL-STD-1388-1 (NAVY) Military Standard 15 Oct 1973
Notice 1 7 Jun 1976
Notice 2 15 Apr 1978

Logistics Support Analysis

- Comment: This document specifies the means by which total logistics support for a system (and its component parts) is established.
- Testability of a replaceable unit or assembly and its testability prediction are directly influenced by the logistics support analysis and the maintainability and support methodology selected for a given system. The document makes no specific reference to testability or testability prediction. (No exhibit.)
- Recommendation: Incorporate into this specification the utilization of testability features and testability prediction in performing logistic support analysis.
- Specific recommendations to pertinent paragraphs are listed below.
  - 5.18.13.3.2 Maintenance Task Analysis
    - ADD: (g) Testability prediction as determined as a sub-discipline of maintainability in accordance with MIL-STD-470 (to be revised to include testability) and MIL-STD-(testability) (to be written).
  - Fig. 2, Block 5.18.13.3 Maintainability Factors
    - ADD: *Testability Prediction (4 places)*
  - Appendix A, Fig. 5
    - ADD: a field on card number B04

      4 Testability Prediction

       34-38
  - Appendix B, Glossary
    - ADD: Definition of testability, testability prediction, and a reference to MIL-STD-(testability) (to be written).

3.3.3.4.5 MIL-STD-1388-2 (NAVY) Military Standard 15 Oct 1973
Notice 1 7 June 1976
Notice 2 15 Mar 1978

Logistic Support Analysis Data Element Definition

- Comment: This document defines specific data elements of the logistic system analysis of MIL-STD-1388-1 (NAVY), hence is in effect an inseparable part thereof.

- Recommendation: Modify MIL-STD-1388-2 as follows:
  - Appendix A Logistics Support Analysis, Data Element Titles

    20. Data Element Titles
    ADD: Testability Prediction

  - Appendix B Logistics Support Analysis Data Element Dictionary

    ADD: Testability Prediction (specific format is TBD)

	FIELD FORMAT				
STANDARD DATA ELEMENT TITLE	LENGTH	TYPE	JUST	DECIMAL PLACE RIGHT	
DEFINITION					
DATA ITEM(S)	EXPLANATION				CODE
TESTABILITY PREDICTION	4	N	R	1	(TBD)
Definition (TBD)					
Data Items (None)					

3.3.3.5 Specifications Related Solely by Definitions to Testability - The following specifications contain definitions pertinent to or related to testability, but otherwise have no testability elements. They are referenced for the purpose of maintaining consistency in definition between related or associated disciplines. (No exhibits.)

3.3.3.5.1 MIL-STD-109B Military Standard 4 Apr 1969
Quality Assurance Terms and Definitions

3.3.3.5.2 MIL-STD-429C Military Standard 25 Nov 1974
Printed Wiring and Printed Circuits Terms and Definitions

3.3.3.5.3 MIL-STD-471A Military Standard 27 Mar 1973
Notice 1 10 Jan 1975
Maintainability Verification/Demonstration/Evaluation

3.3.3.5.4 MIL-STD-721B Military Standard 25 Aug 1966
Notice 1 10 Mar 1970
Definition of Effectiveness Terms for Reliability, Maintainability, Human Factors, and Safety

3.3.3.5.5 MIL-STD-1309B Military Standard 30 May 1975
Definition of Terms for Test, Measurement, and Diagnostic Equipment
Maintainability Prediction

3.3.3.5.6 MIL-HDBK-472 Military Standardization Handbook 24 May 1966
Maintainability Prediction

3.3.4 Other Documents Considered

3.3.4.1 Documents Screened Twice - The following documents were rejected for analysis after the second screening. They contain no references to testability at the module level.

- MIL-C-60898(MU) Military Specification 31 July 1969
  Circuit Card Assemblies, General Specification for

- MIL-D-18300G(AS) Military Specification 1 Mar 1970
  Design Data Requirements for Avionic Equipment

- MIL-E-8189H Military Specification 31 Oct 1975
  Electronic Equipment, Missiles, Boosters, and Allied Vehicles, General Specifications for

  - Comment: This document contains numerous testing specifications.

- MIL-E-16400G(NAVY) Military Specification 24 Dec 1974
  Electronic Interior Communication and Navigation Equipment, Naval Ship and Shore: General Specification for

  - Comment: This document contains numerous testing specifications.

- MIL-N-18307F(NAVY) Military Specification 4 Aug 1978
  Nomenclature and Identification for Electronic Aeronautical and Aeronautical Support Equipment Including Ground Support Equipment

- MIL-T-18303(AS) Military Specification 1 Sep 1966
  Test Procedures; Preproduction, Acceptance, and Life for Aircraft Equipment, Format for

- MIL-T-28798A(EC) Military Specification 11 Sep 1974
  Test Set, Digital Module

  - Comment: This specification pertains to a specific digital test set.

- MIL-STD-12C Military Standard 15 June 1968
  Supplement 1 1 Feb 1971
  Notice 1 (Superseded by Notice 2) 15 Jun 1968
  Notice 2 1 Feb 1971
  Abbreviations for Use on Drawings, Specifications, Standards and in Technical Documents

- MIL-STD-1364D(NAVY) Military Standard 30 Sep 1976
  Standard General Purpose Electronic Test Equipment Equipment

  - Comment: This standard lists and categorizes general purpose test equipment.

- MIL-STD-1389A Military Standard 21 Dec 1977
  Design Requirements for Standard Electronic Modules

- MIL-STD-1540A(USAF) Military Standard 15 May 1974
  Test Requirements for Space Vehicles

- MIL-STD-1665 Military Standard 20 Jan 1968
  Test Equipment for the Standard Electronic Module Program

- MIL-HDBK-246 Military Handbook 10 Mar 1978
  Program Managers Guide for the Standard Electronic Modules Program

3.3.4.2 Documents Screened Once - The following documents were rejected for analysis after the initial screening. They contain no references to testability.

DOD-W-83575A (USAF)	MIL-C-46357 (MU)	MIL-C-51387 (EA)
MIL-E-4158E (USAF)	MIL-E-5400R	MIL-F-13926A (MU)
MIL-F-18870E (OS)	MIL-I-983E (SHIPS)	MIL-M-28787A
MIL-M-38510D	MIL-P-11268K (Army)	MIL-P-22630 (Wep)
MIL-P-28809	MIL-P-46843 (MI)	MIL-Q-9858A
MIL-T-8679	MIL-T-21200L	MIL-T-27615A
MIL-T-55523 (EL)	MIL-STD-143B	MIL-STD-188C
MIL-STD-202E	MIL-STD-242	MIL-STD-275D
MIL-STD-280	MIL-STD-461A	MIL-STD-483
MIL-STD-490	MIL-STD-499A (USAF)	MIL-STD-750B
MIL-STD-785A	MIL-STD-788 (SHIPS)	MIL-STD-810C
MIL-STD-883B	MIL-STD-965	MIL-STD-1311B
MIL-STD-1383 (TD)	MIL-STD-1535A	MIL-STD-1552
MIL-STD-1631A (NAVY)	MIL-STD-1634	MIL-STD-1665
MIL-STD-1679 (NAVY)	MIL-STD-2074(AS)	

3.3.4.3 Documents Cancelled - The following document was referenced in another specification but has been cancelled.

MIL-M-23313A

3.4 Current Testability Documentation Activities by Department of Defense, Air Force, Army, and Navy.

3.4.1 Introduction - The Department of Defense and the several service branches are deeply concerned about the problems affecting maintenance of complex electronic systems. They have been and are taking action on a number of fronts to meet these problems head on to resolve them. The purpose of this summary is to make the readers of this report aware of such activities known to the writer, and indicate who are the leaders in these efforts.

3.4.2 Department of Defense and Joint Services

- The Industry/Joint Services Automatic Test Project is the main focal point for this effort. Particular attention is directed to the forthcoming report of Task Group 1C BIT/Design for Testability Committee as being

directly applicable to this report. For information on publications of this project the reader is referred to:

Lenore Stevens
Chairperson, Committee V Publications
Editor/Manager Corporate Technical Publications
Bendix Corporation
Bendix Research Laboratories
Bendix Center
Southfield, MI 48076

3.4.3 Air Force

- Testability Guidelines and Specifications for Avionics and GSE (under development) for Air Force Modular ATE (MATE) Program, Code ADS/AEGB, Wright-Patterson Air Force Base. This is a competitive study being performed under contract by Sperry and Westinghouse. Key Air Force personnel are:

  Lt. Col. R. H. Henscheid ASD/AEGB
  Wright-Patterson AFB, OH 45433
  Telephone (513) 255-6612
  Officer in Charge of the Modular
  Automatic Test Equipment Program (MATE)

  Mr. Gene Wolanski ASD/AEGE
  Wright-Patterson AFB, OH 45433
  Telephone (513) 255-6600
  Mr. Wolanski has excellent knowledge of Air Force activities concerning military specifications.

  Chief M/SGT Red Allen ASD/AEGB
  Wright-Patterson AFG, OH 45433
  Telephone (513) 255-5744
  Sgt. Allen has been working on Air Force testability problems for many years and knows who to contact for information regarding specific activities.

- Rome Air Development Center, Code RADC/RBRT, have several tasks in progress related in some way with testability specifications. Possible knowledgeable contacts are Tony Capola and Jim Saparito. This was reported as a design-to-repair study so no follow-up was made.

- Rik Krupa of Wright-Patterson AFB is familiar with a recent update of Air Force Test Requirements Document.

- AF Avionics Lab.
  Wright Patterson AFB, OH 45433

  - Task is a design-for-repair study from a systems point-of-view; draft report due 15 June, final report due 15 August.

- Floyd Gerkin, Program Manager
  Hughes Aircraft Co. MSG
  CP1-T25
  Canoga Park, CA 91304
  Telephone (213) 883-2400, X2528

3.4.4 Army

- Manufacturing Methods and Technology for "Digital Fault Isolation for Printed Circuit Boards." CONTRACT DAAK-40-78-C-0290 Missile Research and Development Command (MIRADCOM), U.S. Army, in preparation by Hughes Aircraft Co., Ground Systems Group, Fullerton, CA 92633.

  - This is the contract under which this report is being made.

  Technical Representative:
  Mr. Gordon Little
  COTR, DRDMI-EAT
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  Hughes Program Manager:
  Mr. John Romanelli
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  P.O. Box 3310 B607/M304
  Fullerton CA 92634
  Telephone (714) 732-5492

- "Testability Specification", prepared by Army CORADCOM, Code DRDCO-TCS-M, Ft. Monmouth, NJ, 3 Nov 1978, prepared under contract DAAB07-77-C-2727 by Dynamic Sciences, Inc., Van Nuys, CA 91406.

  - Mr. Sam Torrey
    Ft. Monmouth, NJ
    Telephone (201) 244-5507
    (201) 532-5608

  - Mr. John Irwin
    Dynamic Sciences Inc.
    7660 Gloria Ave.
    Van Nuys, CA 91406
    Telephone (213) 782-0820

3.4.5 Navy

- MIL-STD-2084, General Requirements for Maintainability of Avionics Systems (under development) an upgrading of NAVAIR AR-10.

  - Mr. Bucky Walters
    Naval Air Systems Command
    Telephone (202) 692-7593

- Draft MIL-STD on Electronics Testability Requirements (under development). Digital portion prepared by NAVSWC Code F105 and analog portion being prepared by NOSC Code 8254, both for NAVELEX 304.

  - Mr. William L. Keiner
    Code F105
    Naval Surface Weapons Center
    Dahlgren, VA 22448
    Telephone (703) 663-8586

    Bill Keiner has excellent cognizance of testability activities both in the Navy and in the other services. He has been a great aid in helping collect this data.

- Underwater Weapon Design-for-Testability Specification Guidelines, Naval Underwater System Center Code 3644, 5 Oct 1978.

- Test Point Selection Standard (under development). An upgrading of Navy MIL-STD-1326 by NAVMAT 04T.

- Mr. Arnold Greenspan of AMG Associates has been working with some branches of the Navy on testability problems, as well as having very good familiarity with the overall testability field.

  - Mr. Arnold Greenspan
    President, AMG Associates
    1515 So. Jefferson Davis Hwy, Suite 204
    Arlington, VA 22202
    Telephone (703) 998-5757

APPENDIX I

1.0 The exhibits that follow are for the purpose of amplifying and illustrating the comments and recommendations made in the body of paragraph 3.0 of this report. They are not complete documents. Paraphrasing, extractions and elisions have been freely used to reduce the length of the text while still retaining the desired essence of the context. If any conflict exists between an exhibit and the source specification, the applicable source document prevails.

This appendix consists of the following exhibits:

3.3.3.1.1 AR-10A Maintainability of Avionic Equipment and Systems

3.3.3.1.3 MIL-STD-1326(NAVY) Test Points, Test Point Selection, and Interface Requirements for Equipments Monitored by Shipboard On-Line Automatic Test Equipment

3.3.3.1.4 MIL-STD-2076(AS) Unit Under Test Compatibility with Automatic Test Equipment, General Requirement for

3.3.3.1.5 MIL-STD-2077(AS) Test Program Sets, General Requirements for

3.3.3.2.1 MIL-E-11991D(MI) Electronic, Electrical, and Electromechanical Equipment, Guided Missile and Associated Weapons Systems, General Specification for

3.3.3.2.2 MIL-M-24365(SHIPS) Maintenance Engineering Analysis: Establishment of, and Procedures and Formats for Associated Documentation; General Specification for

3.3.3.2.3 MIL-STD-1519(USAF) Test Requirements Document, Preparation of

3.3.3.2.4 MIL-HDBK-239(NAVY) Navy Standard Electronic Module Program Application Handbook

3.3.3.3.1 MIL-T-24309(SHIPS) Technical Support Plan for Electronic Equipment

3.3.3.3.2 MIL-T-28800B Test Equipment for Use with Electrical and Electronic Equipment, General Specification for

3.3.3.3.3 MIL-STD-1378B Requirements for Employing Standard Electronic Modules

3.3.3.4.1 DOD-E-8983C Electronic Equipment, Aerospace, Extended Space Environment, General Specification for

3.3.3.4.2 MIL-STD-454 Standard General Requirements for Electronic Equipment

EXHIBIT 3.3.3.1.1

AR-10A Naval Air Systems Command, Department of the Navy 1 Jan 1969
Maintainability of Avionic Equipment and Systems

- Comment: MIL-STD-2084 (pending) will obsolete AR10A. A preliminary copy has been solicited.

1 SCOPE

1.1 Purpose. This document specifies the maintainability and built-in test requirements for avionic equipment.***

(c) The Maintainability Program Plan (see 3.2)

(d) Built-in-Test (BIT) Function (see 3.3)

(e) Maintainability Indices and Requirements (see 3.4)

(f) Test Points (see 3.5)***

(h) Maintainability Analysis and Tests (see 4)***

3.1.1 VAST Compatibility. (Required unless contract or order otherwise specifies); see AR8.

3.1.3 Modularization***

(2) (dispose-on-failure trade-off factors (including fault isolation) and cost/MTBF non-repairable criteria).

3.1.4 Standardization (minimum of part, component, and module types to ease testing and spares requirements at all maintenance levels)

3.2 Maintainability Program. (contractor shall conduct using MIL-STD-470 guide and record plan subject to audit)

3.3 Built-in-Test (BIT) Function. Suitable BIT features shall be incorporated into the system or equipment to provide both a failure detection function and a failure location function. (Applies to WRAs per para 3.3.3.)

3.3.1 Failure Detection Function. (Pertains to equipment level testing.)

3.3.2 Failure Location Function. (Pertains to fault location to WRAs.)

3.4 Maintainability Requirements. (Primarily pertains to design requirements for maintainability.)

3.5 Test Points. Test points shall be provided on the equipment for all levels of maintenance (compatibility of test points with test equipment and test programs).

3.5.1 Functional Test Point Selection. Test points shall provide safe and convenient access to electronic circuits. This access to the circuits shall enable performance of the following:

(1) Determination or verification of the existence of a fault or performance degradation.

(2) Localization of the fault to the degree needed for efficient repair.

(3) Checkout of the equipment to ascertain that the fault or degradation has been corrected.

3.5.2 Functional Test Point Arrangement. (Specifies type, location, grouping of test points.)

3.5.3 Organizational Maintenance Test Points. (Establishes requirements for and purposes of test points for Organizational Maintenance (WRA and above).)

3.5.4 Intermediate and Depot Maintenance Test Points. (Establishes requirements for shop test points to isolate fault to SRA; and SRA test points to isolate fault to non-repairables within the SRA.) (This is the plug-in card level.)

3.6 Design Data and Reports. (Required only if specified by contract.) (Includes maintainability program plan, test philosophy and support equipment proposed, maintainability prediction, system top-down breakdown and established repairability for each element with other pertinent data; final report.)

4 QUALITY ASSURANCE PROVISIONS. (Methods used to verify compliance.)

6 NOTES:

6.1 Definitions. WRA, (LRA, HRA), SRA (QRA, BRA, IPRA), SUB-SRA; levels of maintenance; operational readiness test.)

EXHIBIT 3.3.3.1.3

MIL-STD-1326(NAVY) MILITARY STANDARD 15 Jan 1968
Notice 1 1 Apr 1969
Test Points, Test Point Selection, and Interface Requirements for Equipments Monitored by Shipboard On-Line Automatic Test Equipment

1 SCOPE

1.1 Scope. This standard establishes the requirements for providing test points in prime equipments for monitoring by on-line automatic test equipment (ATE) ***

1.1.1 Application. The requirements of this standard are applicable to the design of equipments intended to be interfaced with ATE. ***

3 DEFINITIONS

3.1 *** The following definitions are defined as related specifically to this standard.

3.1.1 ATE. An abbreviation of the term "Automatic Test Equipment".

3.1.2 Prime Equipment. An equipment or system that is to be monitored by ATE.

3.1.4 ATE Test Point. A sensor output which is brought to an accessible location for connection to ATE.

4 GENERAL REQUIREMENTS

4.1 Purposes of Test Points. ATE test point signals will be utilized to provide an indication of equipment performance and to permit fault location to the replaceable module or functional entity. *** A sufficient number of test points shall be provided to facilitate the location of the most probable type of circuit malfunctions which may be reasonably expected to occur. ***

4.5 ATE Input Impedance. Each ATE test point signal output shall be capable of driving a capacity load of up to 1000 picofarads in parallel with the ATE resistive load of one megohm.

5 ATE MEASUREMENT CAPABILITY

5.1 General. The ATE will have a capability to make the following types of measurements. ***

(a) Dc voltages

(b) Pulse parameters

(c) Time interval

(d) Frequency

5.3 AC Voltage Measurements.

5.3.1 Conversion. Prime equipment ac voltages chosen to be monitored shall be converted by sensor to a proportional dc voltage.

5.3.2 Measurement. After conversion to dc by the sensor, the dc voltage measurement specifications *** shall apply.

6 TEST POINT SELECTION

6.1 Philosophy. Circuit test points shall be selected on their ability to select and isolate faults with a maximum degree of confidence to the lowest level practical at minimum cost.

6.2 General Test Point Criteria. Circuit test point placement shall be such that the degree of automatic testing reflects the repair philosophy dictated by physical configuration of the design. Since two types of repairs are possible, piece-part and module replacement, it is necessary to approach these problems differently. ***

6.2.5 External Power Monitoring. A separate ATE test point, with a DC type output, shall be provided to monitor each equipment primary supply voltage from external sources. It shall monitor presence of voltage *** .

6.2.6 Mode Monitoring. A separate test point shall be provided to monitor each normal mode of operation or condition that can be selected by an operator. ***

7.2 Test Point Data Sheet. A list of all ATE test points shall be prepared *** (detailed instructions for preparing the data sheet follow).

7.3 Recommended Test Logic. A separate test logic chart shall be submitted for each normal mode(s) of prime equipment operation that has a unique selected group of test points to be monitored. *** (Instructions for organizing the chart follow.)

8 DESIGN REVIEW CONTROL

APPENDIX - DISCLOSURE FORMATS

10 INTRODUCTION. (Description of formats for a system of diagrams to disclose each level of system design.)

20 BLOCK DIAGRAM. (Details of requirements follow.)

EXHIBIT 3.3.3.1.4

MIL-STD-2076(AS) Military Standard 1 Mar 1978
Unit Under Test Compatibility with Automatic Test Equipment, General Requirement for

3 DEFINITIONS. (Of WRA, SRA, SSRA, UUT, TPS)

4.1 Defines ATE compatibility.

4.1.2, 4.1.3, 4.1.5 - Defines failure for WRA, SRA, Sub-SRA

4.1.2, 4.1.4, 4.1.6 - Specifies diagnostic fault isolation requirements for WRA, SRA, Sub-SRA.

5.1.1a - Lists some conditioning circuits for UUTs to facilitate transmission and measurement of test information.

5.1.1.d - Lists some compatibility design guides.

5.1.2 thru 5.1.2.6 incl. - Specifies test point requirements.

6.1.1.1g and Appendix B - Specifies a means of quantitatively measuring the adequacy of the UUT design relative to ATE compatibility requirements.

Appendix B - Compatibility Task Scoring Data - a quantitative method for matching ATE and UUT design.

Appendix E - Provides means for accounting for fault diagnostic ambiguity groups versus fault isolation design criteria in the contractual document.

Appendix F - Provides means for establishing fault isolation data to meet the fault isolation test requirement for differentiation between good and faulty UUTs, means to locate a fault, and to effect necessary repair.

References a forthcoming MIL-STD proposed (AS) that defines WRA, SRA, and Sub-SRA.

EXHIBIT 3.3.3.1.5

5.1.1.2 Self-Test Survey. The self-test survey routines are designed to test the most stringent and critical ATE resources that will be required by the TP. ***

5.1.1.3 Identity Checks. The identity checks shall verify that the UUT-ID combination and their interconnection is correct. ***

5.1.1.4 Safe-To-Turn-On Test. Safe-to-turn-on test shall be provided *** .

5.1.1.5 Performance Routines. The performance routine shall consist of discrete tests designed to automatically detect and annunciate the presence of any malfunction within the UUT *** .

5.1.1.6 Diagnostic Fault Isolation Routine. The Diagnostic Fault Isolation (DFI) routine shall isolate and identify the fault(s) detected by the performance routine(s).

5.1.1.6.1 Design Requirements. The DFI routine shall perform fault isolation to the next lower levels of assembly.

5.3 ATE Communications. All directions to the operator for operator actions required during the running of the TP and the final diagnosis shall be displayed on the ATE display or Printing Device. ***

5.6 Utilization of BIT and BITE. UUTs designed to include BIT and BITE circuitry shall be tested in a manner that makes efficient utilization of these testing aids. ***

5.7 Test Program Instruction. The contents of the TPI shall contain that information which cannot be communicated by the ATE and is required to accomplish testing of the particular UUT. ***

5.7.1 Physical Requirements. The TPI shall be provided in hard copy.

5.9 Interface Device. It is a requirement to minimize the complexity of IDs subject to the following rules:

a. Optimize IDs so that as many UUTs as practical can be tested by the same basic ID assembly *** .

b. Each ID shall have a minimum Mean Time Between Failure (MTBF) of 1000 hours *** .

c. Each ID shall be small enough to permit both the ID and any UUT to be physically supported by the intended ATE work surface. ***

5.9.1 ID Types. The following are definitions of simple, intermediate and complex IDs:

a. Simple. The ID is a connection device only. ***

b. Intermediate. The ID is complex in mechanical or electrical design. *** Simple wave shaping, synchronization, and generation may be accomplished in the ID. ***

c. Complex. The ID is used to establish complex synchronization, wave shaping, or signal generation.

5.9.2 Maintainability. *** The IDs shall be designed to be tested on the ATE in the same manner as a normal UUT, except that no additional ID shall be required. ***

5.9.2.1 ID Test. (Details of test requirements for IDs.)

5.9.3 Weight. The weight of that portion of the ID including cables that must be fastened to the ATE shall not exceed 40 pounds. ***

5.10 Drawings and Documentation

5.10.1 Test Program Set Documentation. Each TPS shall have deliverable documentation which consists of Program Design Data and an Interface Device Data Package.

5.10.1.1 Program Design Data (PDD). The PDD shall be the source documentation for the TPs and as such shall consist of the four items discussed (below), as well as an updated Test Requirements Document *** .

40. STANDARDIZED MESSAGES - (Requires use of standard messages.)

40.1 Signature Tests. The signature tests verify that the proper ID(s) or UUT(s) are connected to the ATE for the selected test program.

(Examples of standard messages)

40.2 Safe-To-Turn-On Tests. The Safe-to-turn-on tests are provided to detect shorted input lines, that may damage the UUT, or ATE.

40.3 Operator Intervention During Test Program Execution. (Lists common categories of operator intervention.)

40.3.4 Connection of Probes. The use of probes requires operator action. This information should be utilized only when connections/disconnections must be made during the test.

70.1 ATE Language Program Listing. A standard source level program listing of the complete test program *** shall be provided.

70.2 Diagnostic Resolution Table. Fault Isolation is the primary function of a test program. *** To achieve this purpose, DFC fault exit data shall be provided in summary form as a set of Diagnostic Resolution Tables. ***

3.3.6 Operation and maintenance.

3.3.6.1 Simplicity.

3.3.6.2 Ease of operation.

3.3.6.3 Ease of adjustment and maintenance. The equipment shall be so constructed that all parts, terminals, and wiring (other than encapsulated or hermetically sealed modules) are accessible for circuit checking, adjustment, maintenance, and repair with a minimum of disturbance to other parts and with a minimum number and variety of special tools. ***

3.3.6.4 Accessibility. Accessibility shall be in accordance with Requirement 36 of MIL-STD-454.

3.3.6.7 Closed loop circuits. Closed loop circuits shall be so designed that external test equipment can be inserted for routine maintenance and diagnostic purposes.

3.3.16.2 Test points. Test points shall be in accordance with Requirement 32 of MIL-STD-454.

3.3.16.3 Built-in test equipment. Built-in test equipment shall be incorporated to the fullest practicable extent to permit monitoring of performance on a go-no-go basis. *** The built-in test equipment shall enable rapid assessment of performance by semi-skilled personnel. *** The built-in test equipment shall enable test and evaluation of *** modules and plug-in components *** .

3.3.16.4 Accuracy. When test instruments are built into an equipment, they shall be required to maintain their accuracy under all electrical, mechanical and other environmental conditions required of the equipment.

3.3.16.5 Accessibility (test points and terminals). ***

6.3 Definitions. For the purpose of this specification, the following definitions shall apply. (List of peculiar definitions.)

6.3.7 Equipment failure. An equipment failure is the cessation of ability to meet the minimum performance requirements of the equipment specifications *** (and) is not reobtainable through permissible readjustment of operator controls.

EXHIBIT 3.3.8.2.2

MIL-M-24365A(SHIPS) Military Specification 20 July 1970
Maintenance Engineering Analysis; Establishment of, and Procedures and Formats for Associated Documentation; General Specifications for

1.1 Scope. This specification establishes the minimum requirements for contractor performance of a maintenance engineering analysis of proposed and actual designs for maintenance and logistics support of *** assemblies, and subassemblies; and establishes requirements, procedures, and formats for associated documentation.

1.2 Objectives. The objectives of the maintenance engineering analysis are to influence design of systems and equipment toward optimum readiness, performance, and economical support ***.

3.2.1 MEA Selection Criteria
(c) Repairable items where their complexity or essentiality warrants separate identification of logistics resources ***.

3.2.2 Interfaces

3.2.2.1 Maintainability interface. Related maintainability design efforts will influence the Maintenance Concept ***.

6.0 Notes

6.1 Intended Use
(a) As tools for design influence and tradeoffs to enhance supportability.

6.2 Ordering Data. ***

6.2.1 Procurement cycle instructions. It is intended that the MEA can be utilized at any life cycle phase.

6.3 Logistics concepts and parameters ***
(b) Maintenance concepts***
(1) Use of built-in test equipment
(2) Use of automatic fault location ***
(7) Repair or throw-away concept
(8) Modularization concept ***
(12) (level of support planning; skill levels available; new skills required; other constraints) ***

6.4.4 Maintenance Requirement ***
Functional test ***
Fault isolation ***

30.2.3 Maintainability and maintenance concept, worksheet III. Worksheet III utilizes outputs of maintainability engineering efforts ***
(b) Maintainability characteristics
(c) Maintenance concepts

Worksheet II

(4) Probable modes of failure. Briefly describes the primary and secondary modes of failure and their symptoms ***.

Worksheet III

(2) Item Function, maintainability characteristics ***
*** Maintainability characteristics such as *** built in test and fault isolation procedures *** .

Worksheet IV

3. Maintenance requirement.

(7) Functional test. *** At the assembly or module level, functional test includes bench check to verify the need for repair *** or to determine serviceability after repair is completed. ***

(10) Fault isolation. Fault isolation shall apply when the basic intent is to identify the specific item which caused the failure symptom. The fault isolation procedure may include operation of built-in test requirement, self check *** .

4. Maintenance Task

NOTES:

*** (2) Describe troubleshooting tasks in detail *** .
(4) Describe the complete end-to-end troubleshooting task that will isolate probable failures to a faulty replaceable assembly, or replaceable module or part.

EXHIBIT 3.3.3.2.3

4.2.6.1 Electrical Interface ***

c. Test Point Connectors: All test point connectors shall be specifically identified *** so that each test point connector and test point can be located on schematics and other drawings.

5.3 Detailed performance characteristics ***

d. Test point data: The test points shall be identified by function, and the signal (input or output) conditions shall be specified.

5.4 Detailed test information

5.4.3 Guidelines

5.4.3.15 The addition of external feedback loops to the UUT *** shall be avoided and open loop tests made wherever possible. ***

5.4.3.16 All test points specified on the detailed test information sheet shall be identifiable on the UUT schematic.

5.4.3.17 If a test point and a connector pin are electrically common, the connector pin shall be used if it is accessible.

EXHIBIT 3.3.3.2.4

MI-HDBK-239(NAVY) Military Standardization Handbook 5 September 1973
Notice 1 20 August 1976
Navy Standard Electronic Module Program Application Handbook

- Reference is to particular sections of the handbook that can be applied (with some degree of modification) to other module designs and design philosophies.

- Section 4
  Functional partitioning - partitioning methods of paragraph 4.3.1 and 4.3.2 can be applied at the card level.

Logic families	- DTL	4.4.1	4.4.1.1
	- TTL	4.4.2 thru	4.4.4
	- DTL/TTL	Mix	4.4.5
	- MOS	4.8.1 &	4.8.1.1
Schottky TTL,	STTL	4.8.2	
	ECL	4.8.3	
	HCL	4.8.4	
Logic family comparison		4.8.5 and Table IV	

- Section 5
  Module Interface Design - Applies with significant correlation at the card level to mixed logic families and digital/analog hybrids.

  Spacing of test points - 5.7.3.1 technique can be modified to apply to other card families.

- Section 7
  Power Distribution - generally applicable to denser cards at the card level as well as at the card cage level.

  Digital Circuit Guidelines 7.3.1 -

- Section 8
  System test considerations - much of this information is applicable at the card level for denser card families.

  Source Information (pages 115 through 117). The bibliography is from 1962 through 1971. It should be screened for application to current technology and state of the art. An up-to-date bibliography is needed.

- Section 10
  SHP Computer Software - This information is oriented specifically to the SHP program. It would probably require significant modification to be applicable to other card families.

EXHIBIT 3.3.3.3.1

MIL-T-24309(SHIPS) Military Specification 1 September 1967
Ammend 2 (Supersedes Amend 1 6 Sep 1967) 29 December 1967
Technical Support Plan for Electronic Equipment

3 REQUIREMENTS

3.1 General Requirements ***
(a) Maintenance concept
(b) Plan for maintenance ***
(f) Test point and test equipment data

3.2.1.1 Maintenance concept *** (specifies content of maintenance concept).

3.2.1.1 Plan for maintenance (PFM) (delineates specific requirements) *** .

3.2.1.6 Test and test facilities data *** (delineates requirements)

Appendix - Sample Format for Technical Support Plan Report

20 Section I - Maintenance Concept *** (describes required content)

30 Section II - Plan for Maintenance *** (describes required content)

60 Section V - Modular Construction and Assembly Design Data. ***

60.2 (Requirement for test specification and description of required content).

60.3 (Requirement for schematic showing) ***
(c) Description of the following: ***
(2) Test points

60.6 (Requires test equipment set-up drawings)

70 Section VI - Test and Test Facilities Data

70.1 (Include each area requiring test points and support equipment).

70.2 (Schematic diagrams to aid in locating and defining test points) *** .

70.4 (Nomenclature of Military test or support equipment) ***

70.7 Proposed test or support equipment (technical description required)

70.8 (Information on each recommended test facility)

70.9 Test points (requires listing and related technical information)

EXHIBIT 3.3.3.3.2

MIL-T-28800B Military Specification 9 February 1976
Amend 1 20 July 1977
Test Equipment for Use with Electrical and Electronic Equipment, General Specification for

3.4.1.7 Test Provisions
(1) MIL-STD-454 Requirement 32
(2) BIT and self-test capability as practicable.
(3) Test Points - Significant changes in signal and power characters 1000Ω/V AC 20KΩ/V DC voltages
(4) Test Points - accessibility, identification

3.4.1.8.3 - Self-test essential functions
- Fault detection and isolation to piece part
- Short sensing on UUT with disconnect provisions

3.4.3.1 Built in adjustments/compensation to restore to specified tolerance - 1 year

3.11.1 TYPE I Maintainability Requirement 54 of MIL-STD-454

3.11.1.1 Type I Fault Isolation isolation and repair to lowest discrete component

3.11.1.2 Type I Maintainability Demonstration Requirements

3.11.1.4 (c) External accessibility of lamps, fuseholders

3.11.2 Type II Maintainability - same as type III

3.11.3 Type III Maintainability -

3.11.3.1 Type III Fault Isolation - isolation and repair to lowest discrete component

3.11.3.2 Type III Maintainability Demonstration

3.11.3.4 Type III Maintenance Provisions
(a) Accessibility requirement

3.12 Interchangeability

3.12.1 Type I Interchangeability per requirement 7 of MIL-STD-454

3.12.2 Type II Interchangeability - form, fit, function

6.3.2.4 Built-in-Test (BIT) includes BITE & BIT

6.4.2 Ease of Installation and Maintenance - The equipment should be so designed that it can be easily installed and maintained. Accessibility and serviceability features which will lead to simplified maintenance should be a prime consideration in the design.

6.4.5 Reliability, longevity, and maintainability - *** The design should be easy to maintain so as to reduce the requirements for highly skilled maintenance personnel.

EXHIBIT 3.3.3.3.3

Appendix B Testing Philosophy for Digital Modules

30.1.6 RAMs and ROMs. *** Since they are special types of modules, special consideration must be taken when specifying tests. ***

30.1.7 Functional vector set. For complex functions where testing every possible input vector combination becomes impractical, a goal shall be set so that a minimum number of input vectors which detects 100 percent of the internal "Stuck - at" faults shall be included in the detailed module specification.

40.0 DETAILED REQUIREMENTS

40.1 Detailed requirements. Unless otherwise specified, the following tests shall be performed on modules from all sub-families of the digital family except CMOS. Other tests *** may be added. Also, tests may be deleted if they are not applicable. *** (a list of detailed test follows)

40.1.1.6 Functional. Functional test vectors shall check all logic gates in the module for a single stuck-at-one/stuck-at-zero fault. The vectors shall be derived for the actual gate implementation of the circuits used in the module. The goal shall be to detect 100 percent of the observable faults. All vectors necessary to perform the functional tests shall be included in the test table and the test table shall contain both the input and output patterns for each vector.

40.1.1.7 Continuity. (list of where applicable continuity tests).

40.1.1.10 RAM testing. The following 100-percent tests shall be performed on RAM modules.

40.1.1.10.1 Static tests. Static input and output tests shall be performed as stated for all sub-families.

40.1.1.10.2 Write recovery. This is a dynamic test (detailed requirements follow).

40.1.1.10.3 Walking one - walking zero. *** The objective of the walking one - walking zero test (writing a one in a field of zeros and then writing a zero in a field of ones) is to show the independence of each bit in both the zero and one state with respect to all other bits which are in the complement state. ***

40.1.1.10.4 Galloping one - galloping zero. *** The objective of the galloping one - galloping zero test is to test access time. It is necessary to check all possible address transitions (addressing) from a read cycle to a read cycle. ***

40.1.1.11 ROM testing. The following 100-percent test shall be performed on ROM modules.

40.1.1.11.1 Static tests. Static input and output tests shall be performed as stated for all sub-families.

40.1.1.11.2 Functional tests. *** All ROM address locations shall be tested and their corresponding output pattern verified. Verification of the output patterns shall be accomplished by monitoring the outputs and comparing the results with the specified output low and high levels. ***

40.1.2 Sample tests. (Requirements and applicability follow)

40.2.1.15 Functional. *** All vectors necessary to perform the functional tests shall be included in the test table and the test table shall contain both the input and output patterns for each vector. *** Verification of the output patterns shall be accomplished by monitoring the outputs and comparing the results with the guaranteed output low and high levels (or equivalent).

EXHIBIT 3.3.3.4.1

DOD-E-8983C Military Specification 29 December 1977
Electronic Equipment, Aerospace, Extended Space Environment, General Specification for

3.4 Automated design and production

3.4.2 Detailed mechanical and electrical design. The design layout *** (design for producibility to the) specified requirements ***. Redundant components, circuits, etc, in a single enclosure shall be such that a failure in one of the units does not propagate to the other unit. (Use of computer aided design and computer aided manufacturing (CAD/CAM)).

3.8 Operability

3.8.1 Accessibility. Accessibility shall be in accordance with MIL-STD-454, Requirement 36.

3.8.3 Maintainability. The equipment shall be designed so as not to require any scheduled maintenance or repair during its service life.

3.8.4 Durability.

EXHIBIT 3.3.3.4.2

REQUIREMENT 32 MIL-STD-454F

TEST PROVISIONS

1.0 Purpose. This requirement establishes criteria for test provisions.

3.0 Test provisions. Test provisions to provide means for monitoring performance, calibration, and fault isolation shall be in accordance with MIL-STD-415.

3.1 Built-in test devices. Built-in test devices shall maintain their accuracy under all operating conditions. *** These devices shall be provided with *** access for *** checkout or calibration.

3.2 External test points. Protection shall be provided *** to prevent equipment damage caused by the external grounding of test points.

*3.3 Failure effect. Provisions for testing shall be so designed that any failure of built-in test devices will not degrade equipment operation or cause equipment shut down unless equipment is specifically (so) designed ***.

ACCESSIBILITY

1.0 Purpose. This requirement establishes criteria for accessibility.

3.0 Definitions

3.1 Accessibility.

3.2 Part, subassembly, and assembly.

4 Compatibility. Equipment shall be designed for optimum accessibility compatible with operating, maintenance, electromagnetic compatibility, and enclosure requirements.

5 Access. Each article of equipment and each major subassembly forming a part thereof shall provide for the necessary access to its interior parts, *** for adjustment, required circuit checking, and the removal and replacement of maintenance parts. *** For routine servicing and maintenance, unsoldering of wires, wire harnesses, parts or assemblies shall not be required. *** Inspection windows shall be provided wherever necessary.

6 Connections. Connections to parts inside a removable container shall be arranged to permit removal of the container without threading connection leads through the container.

7 Parts. Parts which are identified as replaceable parts for the equipment shall be easily removable and replaceable. *** No unsoldering or soldering of connections shall be necessary when the front panel or any subchassis is removed for maintenance purposes. Design shall be such that where plug-in modules or assemblies are used, they can be easily inserted in the proper location.

8 Enclosures. Accessibility to chassis, assemblies, or parts contained within *** enclosures shall be provided from outside the basic equipment through the use of access doors, *** withdrawal slides, swinging doors, *** which will allow operation in the open position, or other arrangements to permit adequate access. Shipboard equipment shall have complete access for maintenance and servicing from the front of the equipment.

*SUBSTITUTABILITY

*1.0 Purpose. This requirement establishes criteria for the selection and application of substitute parts.

*3.0 Substitution criteria. Except as noted in paragraph 4, substitute parts shall comply with the following:

*3.1 Substitution of parts covered by military specifications and standards that include substitutability or supersession information is acceptable.

*3.2 When the equipment design specifies a commercial part, a military specification part may be substituted when the form, fit, function and characteristics *** are equal to or better than those of the specified commercial part.

*4.0 Initial qualification/reliability demonstration. Substitute parts superior to those specified in the parts list shall not be used in equipment to be subjected to qualification or demonstration tests.

SECTION IVB
DESIGN GUIDE

4.0 Subtask: Testability Design Guide for Digital PCBs.

4.1 Purpose of This Subtask

4.1.1 Statement of Purpose - The purpose of this subtask is to provide a testability design guide for improving the testability digital printed circuit board (PCB) assemblies.

4.1.2 Testability Definitions as Related to Purpose - Though testability has different meanings to different persons[1]; the definition advanced by Keiner and West has been accepted by leaders in the ATE community; it is frequently quoted in the literature:

> "Testability is a characteristic of design which allows the state (operable or inoperable) of a system or any of its subsystems to be confidently determined in a timely fashion."[3]

The proposal for this study advanced the following definition pertinent to a PCB:

> "Testability reflects the susceptibility of a PCB to the detection of all faults, to rapid and accurate isolation to the faulty component without faults, to rapid and accurate isolation to the faulty component without any ambiguity, and to functional test and thereby verification of PCB performance as specified and/or required."[4]

The Testability Subtask Committee of the Industry Ad Hoc Automatic Test Equipment Project for the Navy uses the following definition, which emphasizes the need for consideration of testability early in the design cycle:

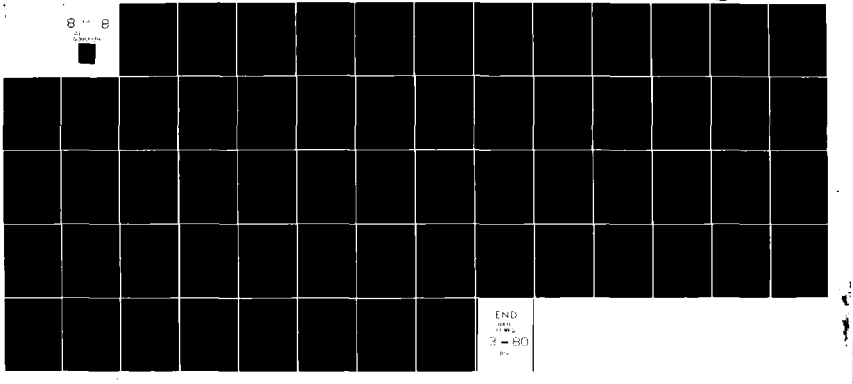
> "Testability is the unambiguous isolation of a fault to an appropriate level of replaceable equipment *** such that proper maintenance is implemented with a minimum expenditure of time and resources. Specification of that appropriate level is a most important consideration, which must be addressed early in the design cycle."[5]

From these definitions and others, it may be deduced that, in Keiner's words: "Just as functional design is concerned with 'how it works', testability design is concerned with 'how it fails'."[2] The objective of this testability design guide then, is to provide rules of design for digital PCBs to enable the detection and isolation of failures in an accurate and timely manner.

4.1.3 Orientation to IC Densities and Logic Families - The testability design guide is oriented to the design of all types of digital PCBs. It therefore requires consideration of all densities of integrated circuits such as SSI, MSI, LSI, VLSI; it includes microprocessor families, bus structured devices, memory devices, and other complex logic geometries. It also includes digital ICs manufactured by all current technologies:

TTL	ECL	NMOS
CTL	DCTL	PMOS
RTL	RCTL	EIA
DTL	HNIL	IIIA
IIL	CMOS	Edge Connector Driver/Receiver

AD-A080 839 HUGHES AIRCRAFT CO FULLERTON CA GROUND SYSTEMS GROUP F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY FOR DIGITAL FAULT ISOLATIO--ETC(U)
AUG 79 DAAK40-78-C-0290
UNCLASSIFIED HAC-FR79-18-669A NL



4.2 How the Report was Developed

4.2.1 Sources of Information - Extensive literature exists on the general subject of testability including means of verifying its achievement, and applying it to fault detection and localization. Much of this literature is published as proceedings of different conferences concerned partly or entirely with testability in its many aspects. Trade magazines regularly have significant articles on testability related topics. A recent publication is devoted solely to testability. Manufacturers of automatic test equipment hold seminars and publish papers and private journals on applications of their products to the solution of current testability problems. Several texts have been published in the resent past, a mere hint of the flood to come. Thus there exists a large, mostly uncollated, body of writings on the subject of interest - testability of digital printed circuit board assemblies.

Information for this report was also obtained from numerous interviews with ATE manufacturers and users, attendance at seminars and conferences, and from past and current testability related efforts at Hughes Aircraft Company.

4.2.2 Initial Screening - A large number of articles were selected by an initial screening process starting from several bibliographies and a reference file of articles. The search extended to proceedings of a number of important conferences, pertinent trade magazines, private publications, manufacturers' journals and applications notes. A list of sources is given in the bibliography.

4.2.3 Classification Into Subtopics - A second screening of the initial selection was done for two reasons, first to cull out papers that, on more thorough examination, were not germane to the study or covered substantially the same ground as a paper previously selected. The second, and more important reason, was to classify the papers as to main content, and from this to sort the papers into pertinent subtopics. This culling and sorting resulted in a total of 135 papers in eight broad subtopics related to testability. The eight subtopics that constitute the main body of this report are:

1) General ad hoc testability design rules
2) Large scale IC testability rules
3) Test point selection criteria
4) Test fixture, adapter rules
5) Modeling, simulation and automatic test program generation
6) IC and circuit design methods for testability improvement
7) Test philosophy and scenario
8) Management for testability

REFERENCES

1. Keiner, W.L., Naval Surface Weapons Center, Dahlgren, VA, "Testability Design Process." Industry/Joint Services Automatic Test Conference and Workshop, San Diego, CA, 3-7 April 1978, pp 121-123.

2. Ibid. p 123

3. Keiner, W. and West, R., Naval Surface Weapons Center, Dahlgren, VA, "Testability Measure," IEEE, 1977 Autotestcon, pp 49-55.

4. Hughes Aircraft Co., Ground Systems Group. Proposal, Volume 1 - Technical, "Manufacturing Methods and Technology for Digital Fault Isolation for Printed Circuit Boards" Project No. R 783242, FP 78-12-96 78E/E3764-501, 27 July 1978.

5. Subtask A-3 Design for Testability, Final Report. Report of Industry Ad Hoc Automatic Test Equipment Project for the Navy. Vol II Research, Development, Test and Evaluation: Conclusions and Recommendations. U.S. Government Printing Office, 1977, 727-156/1-3, p 35.

4.3 Testability Design Guide Body

4.3.1 General Ad Hoc Testability Design Rules

4.3.1.1 Introduction - These are the common rules developed for SSI/MSI logic especially since 1974, which have received prominent attention in the literature. In general they apply to all types of logic design using any of the various scales of IC density and any of the IC technology families, singly or in combination.

4.3.1.2 PCB Mechanical Design

- Mechanical Design Layout

  - Devise a standard grid layout or set of grid layouts for the PCB so that an entire family of logic cards can be accommodated in an orderly arrangement. This greatly aids in identification of components and in interconnections.

  - Employ a design structure that offers the ability to isolate components and prevent them from interacting with one another.

  - Allow enough space between components and ICs (IC sockets) for insertion of IC clips, test probes, and for maintenance of components. The minimum recommended distance is 4.5 mm (.178 in.).

  - Provide at least two mechanical reference holes on each printed wiring board to allow alignment with standard jigs and fixtures.

  - Use standard parts and limit choice to the smallest possible realistic set to reduce logistic problems.

  - Standardize pin configuration of IC placement. Put the number 1 pin in the same relative position to get a common orientation of all ICs.

  - Identify each IC with its reference designator marked on the PCB in the same relative position. Alternatively, for high density PCBs, provide a board layout drawing clearly showing the location and orientation of each component.

  - Associate pullup resistors on the same board as their driving devices. If the pullup must be on a different board for proper line termination, provide a switchable on-board pullup for stand alone PCB testing.

  - Ensure that device leads are accessible (not recessed) so that IC clips and probes used in testing can make contact with them.

  - Provide access by the test set to any on-board switches, keyboards, or displays so that they can be tested independently. This also allows the test set to provide stimulus for a self-test program and allows it to observe the test results.

- Use logic partitioning where it can be done. Seriously weigh the tradeoffs between improved fault detection and resolution versus performance and packaging efficiency. Partitioning is a very potent way to improve card test because it provides output pins (or test points) for sensing, and input pins (or test points) for driving which will greatly improve card accessibility for test purposes.

- Unused I/O pins or test points can provide access to otherwise unavailable nodes for fault detection and isolation of the faulty components. Seriously weigh the tradeoffs between improved fault detection and resolution versus physical layout and routing. Remember that a testing problem is a repetitive difficulty, whereas a routing problem once solved is resolved.

- Confine each PCB to a single logic function. If two or more small functions are placed on a single board, isolate them by partitioning such that each function can be tested separately.

- Make display devices easy to replace.

- Connector Selection

  - Excluding power and ground pins, limit the number of I/O signal pins to 256. If more pins are required, partition the card into sections of 256 or less that can be tested independently. This allows a much freer selection of ATE.

  - Route signals such that adjacent connector pins can be shorted with no damage to the circuitry. For signal lines that cannot be safely shorted to anything, provide a blank pin on each side of that signal pin.

  - Use zero insertion force connectors for extended connector life, easier PCB access, and to facilitate production testing.

  - Use the top or side edge of the logic board as a mounting edge for a connector which can be used for test or control points. Alternatively, an IC socket can be strategically located for use as test or control points.

4.3.1.3 PCB Electrical Design

- PCB Electrical Layout

  - Standardize pin location of common signals such as power, ground, clock, clock return for a card family. Power pins should be located on the connector ends (board edges).

  - Design the system to use only one voltage in order to avoid potential damage that may result from transients or improper voltage sequences.

  - If more than one voltage is required, segregate multiple voltages to as few card types as possible. Provide adequate separation to prevent accidental shorting with test probes.

- Use a single logic family for the logic design. If more than one logic family must be used, select ones with common power requirements and pin assignments, and common input/output signal compatibility and pin assignments.

- If logic families with a signal interface problem must be used, partition the families so they can be tested individually.

- Select logic devices that are independent of specific clock rates, controlled rise and fall times, and/or specific gate propagation delays.

- Run a complete characterization test study on new type devices to avoid sneaky soft (come and go) problems. Be conservative in designs that use such parts, especially with respect to timing parameters. This rule applies with strong emphasis to complex, large-scale devices.

- Design each card to be a functionally separate package. Otherwise separate multiple functions on a card by partitioning so that each function can be tested separately.

- Subdivide large logic boards (>100 ICs) into smaller sections for easier testing. Separate the Vcc paths or use tri-state logic to allow isolating one section from the others for testing.

- Do not mix digital and analog circuitry on the same card. This does not include simple timing circuits.

- If both digital and analog circuitry must be included on the same board, partition the board into digital and analog portions so that each can be tested separately. Provide the digital/analog interconnections externally via I/O pins.

- Design circuits that do not require adjustments. If adjustments must be incorporated, design the board so that the adjustment can be made and locked during test.

- I/O lines should be TTL compatible. Open collector outputs may be used, provided a pull-up is incorporated in the test adapter.

- Design I/O lines to allow for inevitable shorting by providing current limiting or crowbar protection techniques.

- Design I/O lines and test points to accommodate capacitive loads larger than intended in the system. This enables the PCB to be accommodated by a wider range of test adapters and ATE sets.

- Provide means for external control of each node independent of the associated logic by providing direct access via an I/O pin or a test point. This allows external control of the node for troubleshooting purposes.

- Provide sufficient access to the internal circuit by bringing internal test and control nodes to unused pins on the connector, or to pins on the test point connector.

- Provide simple means for initializing (setting to an initial state) all storage elements, using signals applied to I/O pins or test points. A single direct reset is preferred; a short (≤16 bit) count sequence is acceptable.

- Make display refresh circuitry capable of being disabled, with the refresh cycle then being capable of being controlled by the tester.

- Incorporate built-in-test capability into very large logic boards such that BIT can be initiated by the ATE and the test results can be evaluated by the ATE.

- If access to internal circuitry of a PCB is limited, provide BIT capability on the card that can be initiated and read by the ATE.

- Use display LEDs on the PCB to indicate proper operation of important circuits. Examples are: power supply voltage is O.K., clock is present, a phase-locked loop is locked, etc.

- Use position indication fault indicators and displays such that a good test always results in an "ON" condition. A defective indicator or display then always indicates a fault condition, either due to the input, or of itself (if it is faulty).

- For a critical display, provide an alternate method of testing such as "push-to-test" to provide positive verification of its operation.

- Current requirements and limitations

  - Limit input signal requirements including clock and master clear to ≤20 ma. Provide on-board buffering if more drive capability is required.

  - Buffer clock inputs before they fan out to avoid loading down clock drive outputs.
  - Provide sufficient current capability in high frequency and pulse outputs to drive a low impedance transmission line.

  - Provide current limiting on output lines where there is a likelihood of a cascading of failures, should a single component fail.

  - Do not tie direct set or reset lines to Vcc or ground. Decouple Vcc through a resistor to provide a logic high; pass a decoupled high through an inverter to provide a logic low. This protects against shorting Vcc to ground due to a component failure. (See figure 4.3.1-1.)

  - Alternatively use a grounded input inverter to provide a logic high, and a second inverter driven by the first to provide a logic low. This greatly aids in locating a fault due to a shorted fixed "zero" or fixed "one" input.

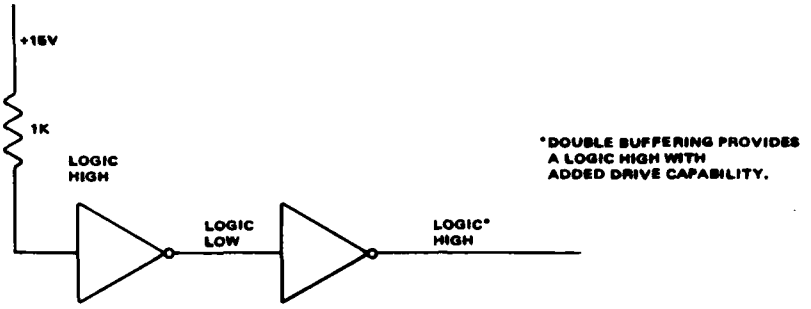


Figure 4.3.1-1. Isolate logic highs and lows from power buses.

4.2.1.4 Redundant Circuitry

- Avoid logically redundant circuits. A connection in a circuit is said to be redundant if no change occurs in the output of the circuit when the connection is open. See figure 4.3.1-2.

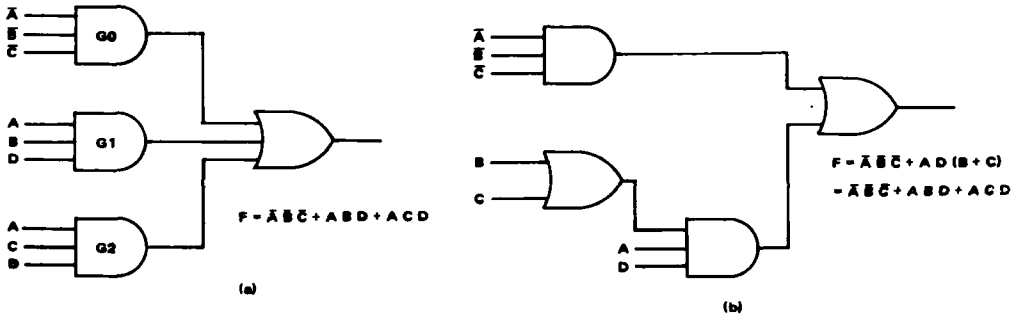


Figure 4.3.1-2. Provide test access by redesign to avoid fault redundancy.

Both circuits generate the same logic function. However circuit (a) gives the the same output even when the B input on gate G1 is stuck at 1, or the C input on gate G2 is stuck at 1. In either case the output becomes $F = \overline{ABC}+AD$, hence the fault cannot be isolated to a specific gate.

With either B or C stuck at one, circuit (b) output also becomes $F = \overline{ABC}+AD$, but now the fault can be isolated to the B*C gate.

- Logically redundant circuits can help solve race problems by providing overlapping control at a clock time.

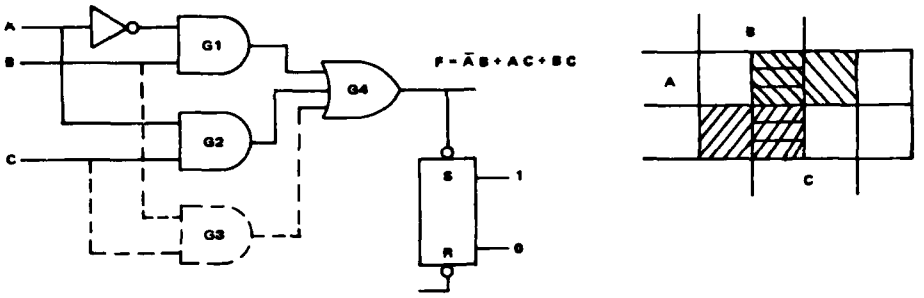


Figure 4.3.1-3. Redundant design can prevent a glitch.

Gate G3 is redundant, as can be seen on the Veitch diagram. However, without G3, a glitch could occur at F during the crossover time between when gate G2 (A•C) releases control and when gate G1 (A•B) takes contr' (or vice versa). The glitch could direct set the flip-flop. By adding the redundant gate G3 (B•C), the glitch cannot occur.

- Some designs, such as majority vote logic, specifically require the use of fully redundant circuitry. Provide access so that each redundant element of a net can be excited and detected independently of the others.

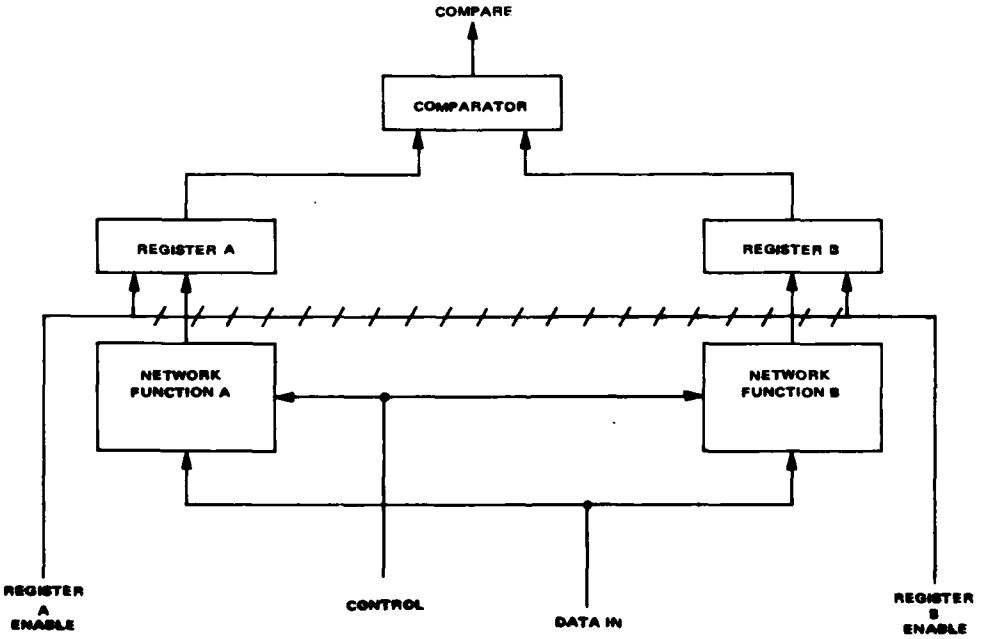


Figure 4.3.1-4. Separate enables allow separate testing of redundant voting networks.

Provide separate enables for registers A and B to allow independent testing. This allows several modes of control for redundant uses.

4.3.1.5 Wired AND and Wired OR Connections

- Do not use wired AND or OR because of the ambiguity that is created in trying to localize a fault to the specific faulty gate.
- Do not use wired AND (OR) with high powered TTL or Schottky TTL; they cannot be direct driven low safely for more than 1 second.
- Break wired AND connections into smaller ambiguity groups as illustrated, figure 4.3.1-5. The before case shows six gates were ANDed; the after case shows three pairs of wired ANDed gates. The ambiguity factor has been reduced from 6 to 3.

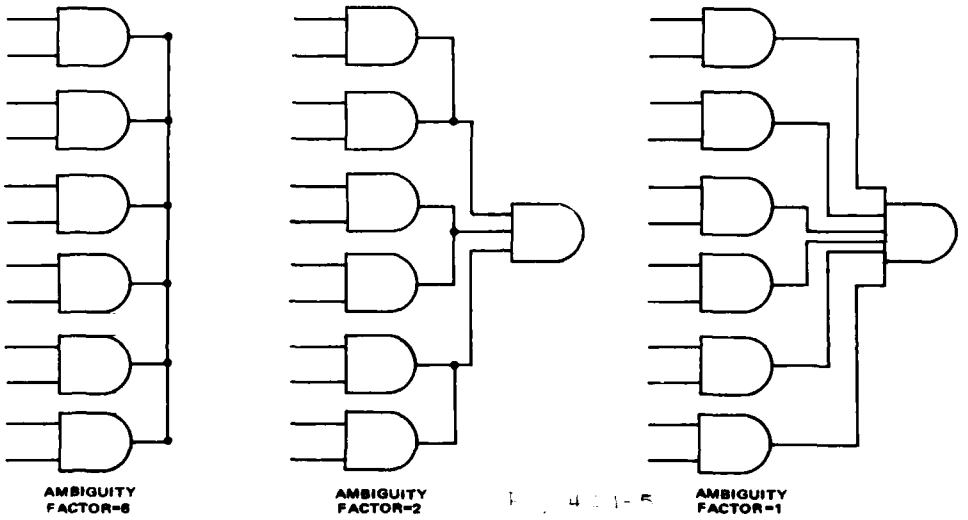


Figure 4.3.1-5. Redesign gate networks to reduce fault ambiguity factor.

- Use wired AND (OR) for external control connections as a means of injecting test stimuli into card under test.

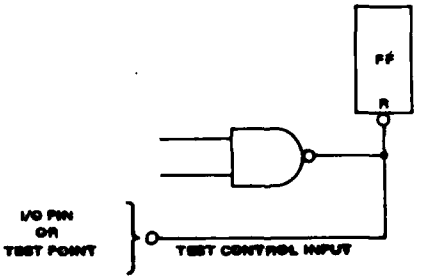


Figure 4.3.1-6. Wired OR for test control input.

4.3.1.6 Internal Clocks and Counter Chains

- Use synchronous clocking systems only. This reduces potential timing hazards to narrow and easily identifiable areas of logic. With synchronous clocking the typical digital logic assembly can be tested on a static digital test system with less concern about timing response.

- Provide an easy means of disabling or bypassing on-board clocks (oscillators, etc) so that the necessary clock stimuli can be provided from the test equipment. Some useful techniques are shown below.

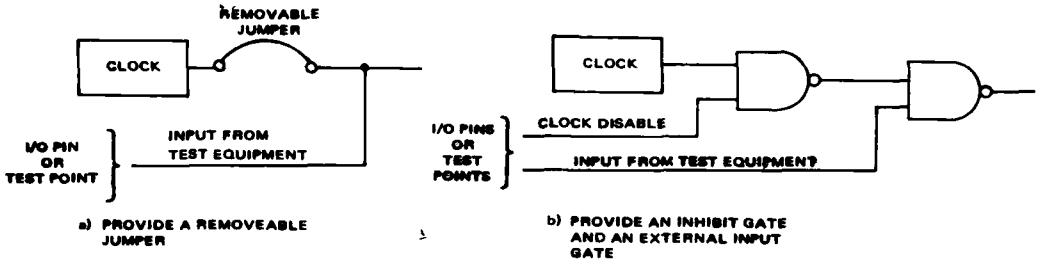


Figure 4.3.1-7. Techniques for disabling on-board clocks to allow off-board clocking.

- Provide means for easily inhibiting an on-board oscillator (putting it into a non-oscillatory mode).

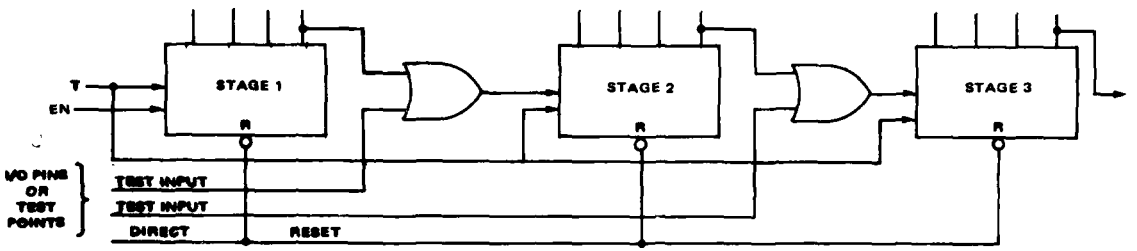
- Always generate multiple clock frequencies by counting them down from a common oscillator. Multiple on-board clocks from unsynchronized oscillators cause both jitter and potentially unstable operation.

- To detect dynamic problems, it is necessary to run the PCB at its normal clock rate in a system emulation. Assuming a thorough dynamic test of the breadboard, and a comprehensive incoming inspection screening of chips, dynamic problems should be minimal at the card level. Economic considerations usually dictate that detection of the rare occurrences be left to system test.

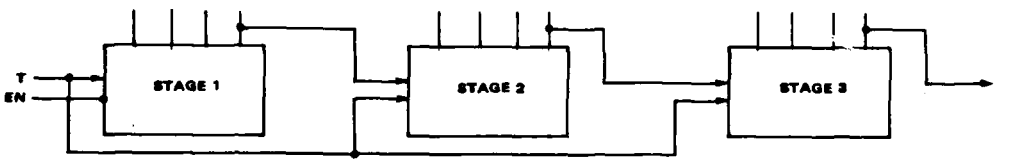
- The most common operating mode is to synchronize the UUT to the test system. This gives the greatest possible level of control since the pattern rate can be accurately programmed. Any on-board clock must be disconnected from the rest of the board. If this cannot be done, then it may be necessary to slave the tester to the clock, or to a clock derived signal on the board.

- Document dynamic clock nodes that require a minimum rate to prevent loss of data.

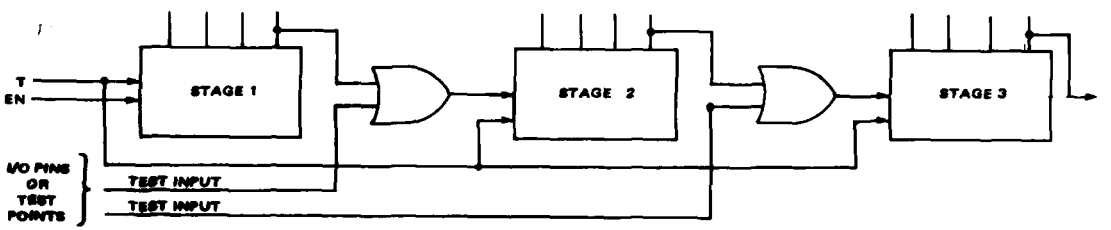
- Break up long counter chains into smaller segments, preferably of equal length, such that the total count time provides a reasonable total test time. See figures 4.3.1-8.



a) MORE IMPROVED COUNTER CHAIN. TEST TIME IS $2^{n/3}$ AND DIRECT RESET IS ACCESSIBLE TO THE TEST SET



a) UNDIVIDED COUNTER CHAIN. TEST TIME IS $2^n \times T$



b) IMPROVED COUNTER CHAIN. TEST TIME IS $2^{n/3}$

Figure 4.3.1-8. Subdivide counter chains to improve their testability.

- To subdivide a counter chain into practical length test sections; (1) provide it with a test input from an I/O pin or a test point, or (2) provide access to clocks and direct resets at I/O pins or test points. See figure 4.3.1-8.

4.3.1.7 Sequential Circuits

- Initialize all sequential circuits to a known start condition utilizing the shortest possible sequence, ideally one transition, and never more than 20 transitions.

- Provide means of initializing all sequential logic elements from I/O pins or test points. This applies to flip-flops, counters, registers, memories, etc. See figure 4.3.1-9. (See also wired AND, wired OR, para 4.3.1.5.)

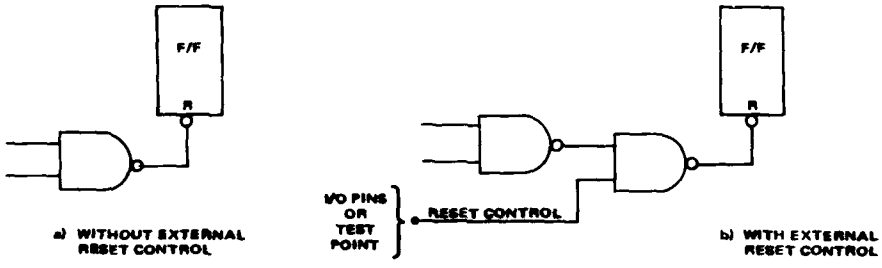


Figure 4.3.1-9. Flip-flop modified for external reset control.

- If an I/O pin or test point is not available, provide initialization by means of "power-up" as shown in figure 4.3.1-10.

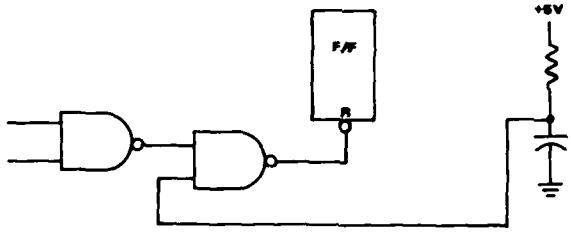


Figure 4.3.1-10. Power-up reset.

- If unused direct reset and set pins must be tied down; always do so through a decoupling resistor. This can make these inputs available for test purposes, and prevents shorting the power bus through a bad chip.

- Latch flip-flops are strongly preferred to edge-triggered flip-flops because of their superior noise immunity and easier testability. When a latch is driven by a constant active clock and enable, it becomes a combinational network.

- Use latch flip-flops only for storage in complex networks such as adder arrays. They can be easily tested as combinational logic, even when input and output latches are in the test path.

- Avoid arbitrary use of edge-triggered devices such as D flip-flops and J-K flip-flops. They increase modeling requirements, yield lower test quality in nodal-fault testing, and often exhibit race conditions.

- Provide access for test control to internal nodes of complex sequential circuits by means of gates, I/O pins, and/or test points. See figure 4.3.1-11.

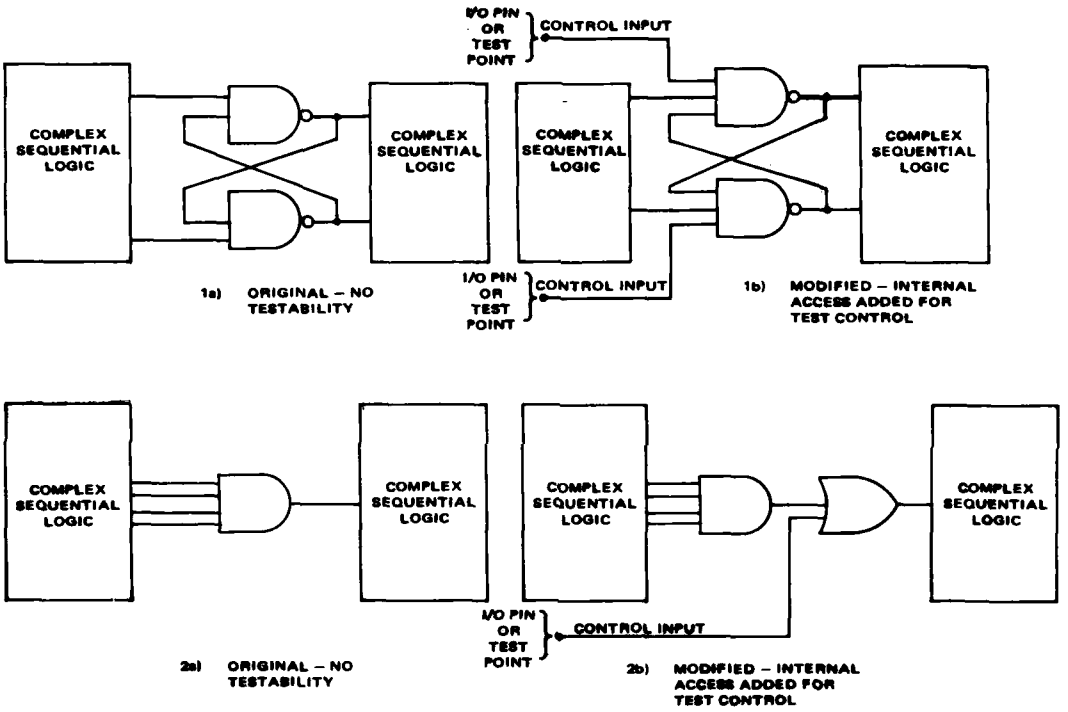


Figure 4.3.1-11. Provide access to internal modes for test control.

- Provide positive controls to prevent logic lockups that can be cleared only by a master clear, or indeterminate outputs such as can occur from an R/S flip-flop.

- Logic designers should provide state diagrams for sequential logic circuits. This will enable the test engineer to analyze tests from valid sequences only, and to ensure that initialization prevents the occurrence of invalid sequences and lockup.

4.3.1.8 Asynchronous Circuits, Monostables (One-Shots) and Feedback Networks.

- Do not use asynchronous clocking. It typically requires use of edge-triggered flip-flops, monostables (one-shots) and/or delay elements to control the functional sequence. Testing monostables and delay lines usually requires manual test generation for accurate timing tests, voiding the use of automatic test generation.
- Asynchronous clocking is highly undesirable because it usually results in the use of various asynchronous clocking methods distributed throughout a functional module. This, in turn, establishes a need for a multitude of separate test environments and extensive costly manual test generation.
- Do not use asynchronous circuits. If they must be used, provide means for synchronizing them in test, or provide means so that they can be tested by themselves.
- Do not use monostables on digital logic boards.
- If monostables must be used, they must be capable of producing synchronized, predictable, and repeatable pulses.
- If use of a monostable is mandatory, provide means of electrically disconnecting the circuit input and output by gating or by jumpers. Provide a path for external test stimulation of the monostable and a test point to measure the monostable output.

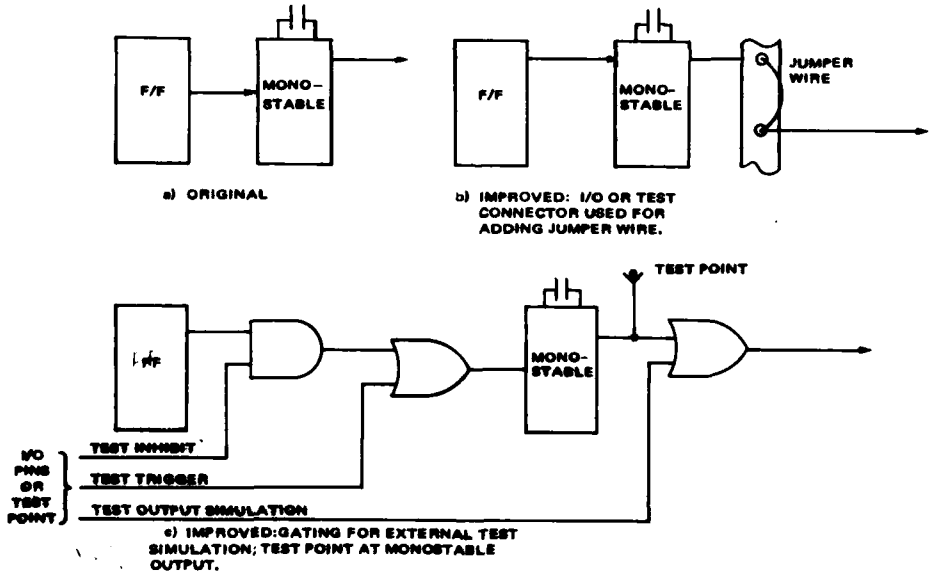


Figure 4.3.1-12. Electrical disconnection of monostables with external simulation path provided.

- Do not use asynchronous feedback networks. Particularly avoid those dependent upon propagation delay. Replace such a circuit with a synchronous feedback function.

- Provide means of breaking all feedback paths so that faults in the feedback loop can be isolated. Ensure that the circuit can be operated in the open loop mode by providing an alternate test input at the place where the loop is opened. Use a jumper wire or gating to open the feedback path.

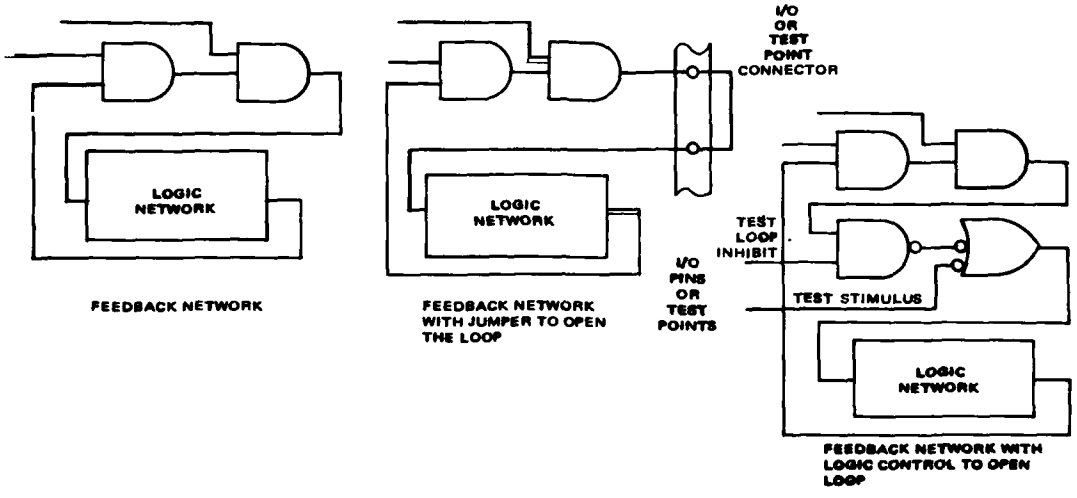


Figure 4.3.1-13. Break feedback paths.

4.3.2 Large Scale Rules

4.3.2.1 Introduction - The large scale testability design rules are those that apply particularly to LSI, VLSI, VVLSI devices including microprocessors, microprocessor support chips, RAMs and ROMs, UARTs, etc.

The ad hoc rules of 4.3.1 apply in general to large scale devices, when appropriately modified to meet the special conditions applicable to such devices. The rules below are those particularly applicable to design using large scale devices.

4.3.2.2 General Rules

- The card designer and the test engineer must both have detailed knowledge of large scale components and the problems of interfacing between them. This knowledge is required to develop a viable design that includes the testability needed to detect faulty operation and to isolate the fault to a defective component.

- Test each lot of an LSI device to ensure that the device characteristics have not changed. A different lot number of a large scale device, particularly in its early life, can mean differences in characteristics.

- Characterization studies to establish worst case limits of critical parameters are essential for LSI devices. Semiconductor manufacturers generally do not provide information on test vector patterns that best test their devices. They generally only furnish DC and timing characteristics. User experience is that characterization studies are worth their weight in gold.

- Use dynamic devices (dynamic RAM, microprocessors, etc.) only when absolutely required. Provide separate access to the refresh clock at an I/O pin or test point.

- The ad hoc initialization rules also apply specifically to volatile memory elements. Conditional initialization is not acceptable without a controlling override absolute initialization. A predetermined short sequence of clock counts to initialize is acceptable.

- Use partitioning judiciously to separate the functioning elements of a product to improve overall testability characteristics.

- Avoid concentrating many LSI chips on a single PC board. The resulting structure is difficult to test and troubleshoot because of the restricted physical access and the restricted test visibility.

- Utilize chips with power ON/OFF capability to electrically partition groups of chips for independent testing of parts of the PCB one at a time. Then the parts can be combined piecewise or en masse, depending upon interface complexity. This approach greatly simplifies fault localization and applies the proven concept of bottom-up integration PCB testing.

- Mount all large and/or complex ICs in sockets so that they can be removed to allow testing by partitioning.

- When doing characterization studies of an LSI device, know what phase in the life cycle the device has achieved. These phases are as follow:

  - Characterization Phase - tests define the critical characteristics and characteristic limits. Processes and parameters are subject to change as the device matures. Production is low.

  - Prematurity Phase - production is increasing and processes and parameters are more stabilized.

  - Shell Phase - production growth is rapid. Tests are pared to a "shell" of critical requirements and some testing of critical processes. Dedicated test equipment is selected. Competition in production is apparent.

  - Maturity Phase - production has peaked. Dedicated test equipment is used for stationized testing of the "shell" of tests selected in the previous phase. Process control testing is minimal but adequate. Competition is reaching its peak.

- Post-Maturity Phase - the device is turned over to the sustaining production group. Routine testing, based on past learning, is done at minimal cost but with tight control of processes. Prices are fixed. Competition has decreased but also has stabilized.

4.3.2.3 Microprocessor and Support Chip Rules

- Capture the microprocessor design effort for later analysis and use in the test development effort. Include all data derived from the use of design and debugging aids such as an MDA (microprocessor development aid), logic analyzer and/or other design tools, including complete information on all equipment setups, procedures, and results. Use computerized tools to perform this data capture automatically and painlessly.

- In a microprocessor system the functional operating characteristics of the circuit are not necessarily associated with specific hardware components.

- Microprocessor systems generally lend themselves well to ordered partitioning. The average microprocessor system has six unique chips.

- Due to their complexity, microprocessors are very difficult to test when incorporated into a PCB as part of the logic design. If they can be mounted in sockets, this permits removing them for testing separate from the rest of the PCB.

- Use microprocessors from the same family in a multiprocessor configuration, rather than different microprocessors unless there are specific compelling reasons to do so. Multiprocessor configurations developed around a microprocessor family are much easier to test.

- Verify that the microprocessor can be run in the tri-state mode (high impedance state).

- Provide inhibit gates for microprocessor outputs that cannot be put into the tri-state high impedance state.

- Separate bit-slice microprocessors into elementary slices for test control. This permits the use of a much simpler program to test each elementary slice independently. Interslice coupling can then be tested by a relatively simple test program.

- Tie unused CPU control inputs to power buses only through resistors or inverters, and provide access through I/O pins or test points. This provides access to the control line for test purposes and prevents shorting of the power bus if the device is defective.

- Microprocessor phase clocks must conform strictly to the requirements of the microprocessor and its associated chips, rather than being dependent upon any other clock circuitry.

- Provide a means to loop I/O port outputs back to inputs for a very effective I/O test. This has been implemented using an on-board test connector together with a test adaptor connector at the board edge.

- The three widely used microprocessor test methods are (1) actual use, (2) stored response from a known good board, (3) algorithmic pattern generation. Actual use test is a naive approach because it usually isn't "actual" use. Rather it tests a very limited subset of the microprocessor's capability, generally under ideal conditions. It may be satisfactory for non-critical applications such as TV games, but is totally unsatisfactory for critical applications such as a brake system failure.

  Stored response from a known good board has two limitations: (1) how was the "known good" board arrived at? (2) the large amount of memory required to store the simulation and response vectors. Microprocessor test times are typically greater than one second. For example, a test pattern with a length of 500,000 clock cycles and 1/2 $sec clock time would require 1/4 sec. for a real time test. Most testers operate slower than real time, and require test vectors numbering in the several millions minimum.

  Algorithmic pattern generation gets around much of the storage requirement and a test result vector compaction method, such as signature analysis, further reduces memory requirements of the tester. The above discussion reduces to the following rules.

  - Use automatic test vector generation and simulation for modeled digital circuitry.

  - Use algorithmic pattern generation to generate test vectors, and a data compaction method (such as signature analysis) to reduce test results vectors prior to storage; and in actual testing prior to comparing with the stored result.

- Testing a microcomputer PCB must start by a thorough analysis of, and test development for, each of its component devices. The logic of this approach is that proof of the satisfactory performance of each component of the microcomputer should be assured prior to performing a test of the whole system. It is most cost effective to test individual chips at incoming inspection.

- Do not attempt to devise microprocessor system tests with the same type of approach as traditionally used for SSI/MSI PCBs. The result will be millions of random test vectors and an unacceptably long test time. The methods of testing previously relied upon are not practical when applied to microprocessors.

- Divide the board into two sections consisting of a non-CPU section and a section containing the CPU and its support chips (clock generator, bus controller, buffers). The non-CPU section contains standard peripheral I/O devices, random standard logic, and often, analog circuits. Figure 4.3.2-1 illustrates this organization.

- Utilize a progressive or structured test plan such as shown in figure 4.3.2-2 for testing microprocessor based PCBs.

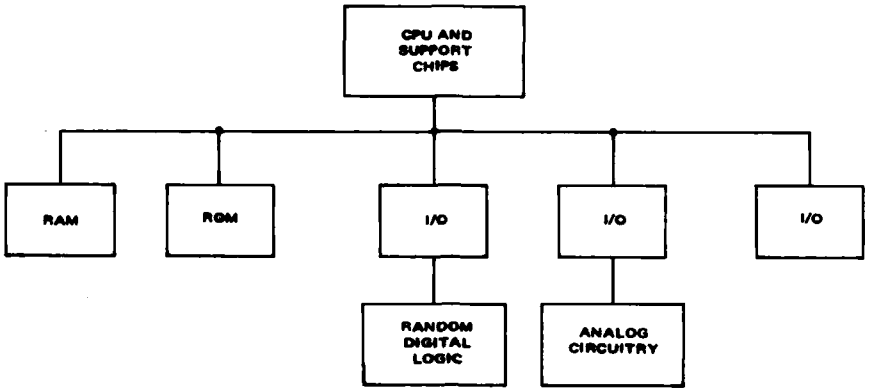


Figure 4.3.2-1. Structure Diagram of Microprocessor Based System

TEST GROUP	TEST SEGMENTS
PRELIMINARY	PCB IDENTITY CONTINUITY (SHORTS, OPENS) BUS SHORTS
STATIC	NON-CPU CPU UNMODELED DEVICES ANALOG
CLOCK RATE	DYNAMIC LOGIC INDIVIDUAL FUNCTIONS SYSTEM EMULATION

Figure 4.3.2-2. Structured Test Plan

- Test the clock circuit immediately after POWER UP tests. An absent, jittery, or noisy clock can play havoc with the rest of the hardware functions. Aberrations of the clock signal may prove fatal, and marginal operation often leads to hard-to-find transient problems.

- Use progressive testing to verify the hardware, employing simple programs. The best test sequence is Power, Clock, ROM, RAM, thorough test of I/O ports and interrupts, and bus control logic.

- Test non-CPU circuitry independently by tri-stating the CPU and utilizing the inhibit gates to isolate the CPU from the other circuitry.

- Perform passive preliminary tests to be sure that the board is free for communication.

- Subdivide the microprocessor into functional units (adder, multiplier, incrementer/decrementer, program counter, input buffer, output buffer, stack pointer, register address, etc.). Devise a diagnostic fault detection only test for each of these units, since they cannot be repaired. Utilize the principle of "expanding on the kernel" in devising the sequence of these tests.

- The principles of individual functional subunit testing and expanding-on-the-kernel provides a controlled progressive means of developing programs. It keeps one from being overwhelmed by the complexity of the device.

- Devise a test for the microprocessor kernel, the minimum configuration of microprocessor and ROM needed to run a very simple test program. Use this proven part to expand testing to an untested area. Continue this test expansion process until the complete microcomputer system has been tested.

- Properly designed-in testability can significantly simplify testing of microcomputers. Three reasons support this conclusion: (1) resident self-test programs written in the microcomputer's own language can be stored directly on ROM. By "expanding on the kernel" these programs provide excellent means for verification of operation, and can easily generate ample stimulus for fault diagnosis. The same self-test can be used for proving out the design in the laboratory, testing in production, and servicing in the field; (2) the system bus, which is centrally located and connects to many components in the system, can be physically designed to provide easy access for application of test stimuli and visibility of test results; (3) bus oriented architectures are inherently readily designed into easily diagnosable modules.

- All software storage locations that are accessed by the CPU must be initialized by an initializing routine that precedes the test routine proper. Include in the initializing sequence RAM locations, peripheral IC registers, input ports, CPU registers and PIAs, etc, that are not affected by hardware initialization. The test designer must be aware of exactly what registers and addresses are saved on the stack at the initiation of an interrupt or subroutine call. When the return is executed these saved registers are read back from the stack into the processor locations, etc, from which they were saved. The initialization procedure must precede any interrupt action or subroutine call to ensure that proper control of these registers, etc, is maintained at all times.

- Microcomputer design should include a built-in self-test, which requires about 1 K-byte of ROM. A software sequence, external switch, or test point can be used for the initiating maintenance action of this test.

- An alternative to built-in test is to utilize an external signal, switch action, or connector to overlay a self-test program onto the applications program RAM memory space, and operate the test from there.

- Write general purpose self-test modules that apply to any system based on a particular microprocessor; for example,a CPU test module and a RAM test module. Usually only small changes are required to adapt the test modules from one system to another.

Write I/O driver routines in applications programs as subroutines so that they can also be incorporated into test routines as a subroutine call. This saves both code space and program development time.

- The first step to localize a microprocessor system malfunction is to determine its generic source. Is it caused by hardware, firmware, or software?

4.3.2.4 Buses

- The first step in functional board test of a microcomputer board is to make sure the bus structure is free of manufacturing faults. This should be done even when the board has been through in-circuit component inspection test (ICCIT).

- Provide access to microcomputer, RAM, ROM (or other device) address, data, and control buses as applicable. This can be done in a number of ways.

  - The most flexible access is to bring all buses to I/O connector pins.

  - Route buses that do not have I/O access to test points (a test connector).

  - Provide space to access the buses by means of a dip-clip. (If the boards are to be conformal coated this is not useful for post-delivery factory retest or for field testing.)

  - Provide access to the control line for tri-state buses at I/O pins or test points.

- The ad hoc rule for putting pull-up resistors on the same board as their driving device, applies particularly to tri-state devices.

- Add a default bus driver to actively pull the bus to a known state when no other bus drive is active. Decode hardware, using address and bus control inputs, is used to generate the default bus control.

- Provide a means for floating or opening each bus line to assist in fault isolation and to allow free running operations. Use one or a combination of the following methods.

  - Hardware or software controlled chip select lines, jumper wires, shorting plugs, socketed components.

  - In multiple board systems, provide a separate extender board with a switch on each data line. Use this board to isolate the suspected board from the others. By closing one switch at a time and observing results, a specific bad bus can be detected.

  - With all data bus switches on the extender open and address bus switches closed, a failure can be localized without the rush of bad data feedback that can invalidate the control test stimulus patterns. Electronic switching will allow the ATE to control the testing and fault detection process.

- Use a current tracing tool to probe beyond the node level. Models are available that can be used off-line to trace the current on a faulty bus line to the source device.

- Do not use multilayer boards where there are bus lines coupling several devices. It is difficult to use a current tracer on such a board to discover which device is holding a bus line high or low.

4.3.2.5 RAMS, ROMS, Serial Registers

- Pattern sensitivity studies must be made for all large scale memory devices. Some current memories use as little as 28% of the real estate for the actual memory area. Circuit features other than the memory array are now primarily responsible for pattern sensitivity.

- Isolate large memory devices (1024 bits or larger) from significant amounts of standard logic. Consider the requirement of special test techniques and equipment for testing large memories.

- Provide access to control (enable) lines and output lines of memory devices at I/O pins or test points. If this is not possible, the memory devices should be mounted in sockets so that they can be removed. This permits a simpler test program for the PCB and a separate test for the memory device.

- Provide means in hardware or software to isolate ROMs from each other and from other bus elements. This can include providing ROM sockets to permit physical removal. This will allow isolation of address decode faults that result in incorrect data being read onto the bus.

- Provide a known PROM output state for every input address combination.

- Define any unused or don't care ROM states such that accidental entry into these states will bring the system back to a defined state.

- Provide means to disable, isolate, or remove each ROM individually in order to isolate the ROMs from each other and from other bus elements. The means can use hardware or software techniques, or a combination.

4.3.2.6 Memory Testing

- Commonly used test patterns are background, checkerboard, stripes, diagonals, parity, walking bits, ping-pong. The applied conditions that are varied are the different supply voltages, 1 and 0 levels, bit timing, cycle timing, etc.

- Schmoo is a term used for a graph which shows the safe margin of operation for one to a number of device parameters. Using appropriate software, different types of schmoos may be displayed and utilized to find device margins.

- Types of schmoos used for testing memories include the following:

  - One- or two-dimensional pass/fail schmoo. All dimensions but those being varied are held constant. The result is plotted as a map or graph with distinct pass/fail indicators. The area included by the pass indicators bound the operating region of the memory.

  - A three-dimensional schmoo is represented by plotting two 2-dimensional schmoos having one common parameter.

  - Cumulative schmoo, obtained by summing n two-dimensional schmoos and plotting the result as a percentage of pass indicators for the n schmoos.

  - Parametric schmoo is a two-dimensional schmoo that displays the value of measurement rather than pass/fail indicators.

  - Class schmoo is a two-dimensional schmoo that displays a pass/fail light at the end of the test, rather than plotting pass/fail indicator symbols.

- Common memory test patterns include the following.

  - MASEST - Load the memory with an alternating 1/0 pattern. Starting at location 0, read all locations according to the following address sequence: location m, complement of m, location m. The resulting sequence is shown in figure 4.3.2-3. Then read the memory sequentially starting at address 0. Load the complement data pattern and repeat the test.

READ 1ST	READ 2ND	READ 3RD
0	$\overline{0}$	0
1	$\overline{1}$	1
2	$\overline{2}$	2
•	•	•
•	•	•
n	$\overline{n}$	n
n IS NUMBER OF WORDS IN THE MEMORY		

Figure 4.3.2-3. MASEST memory test read pattern

- Marching 1's and 0's. Write all 0's into the memory. Read location 0, change it to a 1; increment the address by 1. Repeat this sequence until all address locations have been read. The memory should now be all 1's. Return down the memory starting at the highest address location n. Read n, change it to a zero, decrement the address. Repeat this sequence until all addresses have been read. Repeat, using complemented data.

- WAKPAT - Load the memory with all zeros. Starting at location zero, enter an all 1's test word. Then starting at location 1, verify that all memory locations are zero. Now read the test word, replace it by zeros, increment the address by one. Repeat, writing the test word into location 1, then verify that all other locations are still zero. Restore location 1 to all zeros, increment the address, repeat with location 2. Repeat this sequence until all address locations have been tested. Then repeat the complete test with complement data.

- GALPAT - Enter all zeros background pattern into the memory. Read an all 1's test word into location 0. Perform the following read sequence: location 1, location 0; location 2, location 0; ... ; location n, location 0 (n = number of words). Restore location 0 to all zeros, and make word 1 all 1's. Repeat the read sequence starting at location 2 and continuing through location n, location 0. Repeat this process until the all 1's test word has been written in all locations. Repeat the test, using complement data.

- The following failure modes have been experienced in testing semiconductor memories:

  - Open and short circuits due to metallization; opens due to lack of bondwire contact at pads.

  - Breakdown, due to a clamp diode or other semiconductor function.

  - An input or output leakage current in excess of the specified limit for that current.

  - Inability to address some part of the memory due to a decoder malfunction.

  - Multiple writing which results from data entering more than one cell when only one cell is addressed.

  - Pattern sensitivity which is exhibited by incorrect operation with certain test patterns. These are often discovered in the field, hence emphasize the importance of feedback of field use data.

  - Refresh fault which is exhibited by loss of data when refresh requirements are adhered to.

  - Excessive access time which is exhibited by erroneous data until the access time allowed is in excess of the specified value. This condition usually results from excessive capacitive charge on an output driver requiring an overly long time to sink current.

- Write recovery which is exhibited by excessive access time as read-after-write time approaches the minimum specified value.

- Sense amplifier recovery which occurs when the same data which has been accessed for a number of cycles is suddenly changed, but the sense amplifier tends to remain in the same state as before, rather than following the change.

- Partition memory functions to minimize the number of memory board types. This improves overall testability, by concentrating storage functions in fewer board types.

4.3.3 Test Points

- Select test point locations for maximum access to buried nodes. Strategic placement of test points is far more important than quantity.

- Critical locations for test points are:

  - In feedback loops for control of important signals

  - To subdivide counter chains and long sequential logic paths

  - At wired AND connections and similar high ambiguity paths (fig 4.3.1-5)

  - At points where high fan-out or high fan-in exist (fig 4.3.3-1)

  - On data bus enable signal paths

  - On ROM address lines

  - On chip disable bus lines

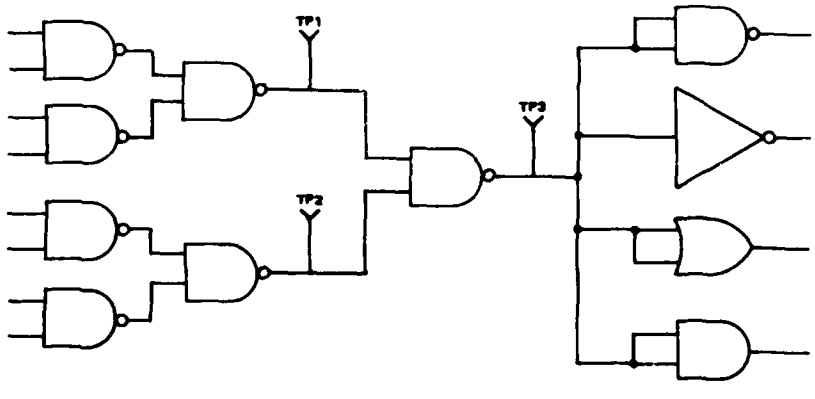


Figure 4.3.3-1. High Fan-Out/High Fan-In Test Point Placement

- I/O connectors located away from the adapter work area. Locate switches for easy access, indicators for high visiblity. Cover all power connections, and ground the adapter to the ATE power ground. Allow room to access both sides of the PCBUT.

- Utilize software controls wherever possible in preference to hardware controls. Software is more readily modified to meet changing requirements and conditions, and does not change due to environmental aging factors.

- Combine similar cards into a sub-family for which a common adapter can be developed. This will maximize the number of card types that can be accommodated by a given adapter.

- Utilize a standard hardware configuration and a standard electrical interface for all adapters employed with a given ATE.

- Select a PCB connector keying system with a built-in defeating mechanism. Then a universal adapter can be used to test many different assemblies.

- Use zero insertion force connectors to interface between the ATE and adapter. The connector interface between adapter and PCB under test should be the same as the using system or a zero insertion force adaptation thereof. This provides extended adapter connector life.

- An alternative to zero insertion force connectors is to use a piggyback connector system. The connector receiving the wear is plugged in to a second connector which, in turn, is wired to the system. The worn connector can be discarded and replaced at small cost.

- Use components within reasonable design capabilities. This particularly applies to higher frequency applications where the physics and engineering aspects of transmission line theory must be considered.

- Use the adapter for interfacing special test equipment such as power supply, signal generator, oscilloscope, spectrum analyzer to the PCBUT. Provide for the necessary remote controlled switching in the adapter by means of relays or plug-in patchboard.

- Utilize switching in the adapter units when high frequencies must be accommodated to minimize path length between the signal source/sink in the ATE and the PCBUT pins. This obviates the need for special cables and critical cable termination design for the majority of frequencies of interest.

- Where data skew is a critical problem, provide a data storage register in the adapter so that the data can be retimed and realigned close to the PCB terminals.

- Input lines may require special hardware modification to adapt to the modeling capabilities of the particular ATE being employed. Particular attention must be paid to differential line receivers.

- Provide appropriate level converters in the adapter to drive the various receivers in the ATE. Appropriate switching in the adapter accommodates these level converters to multiple use.

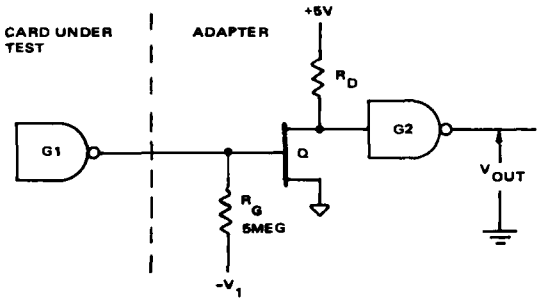
- Locate resistors in the adapter to properly load the outputs of the PCB under test. Provide a nominal seven units of load for each ten units of TTL drive, exclusive of other loading.

- Provide buffers for memory element (latch/flip-flop) outputs to block noise feedback from the adapter into the memory element.

- Provide load resistors for unterminated open collector outputs on the PCBUT.

- Provide open collector drivers to control wired-OR/wired-AND junctions terminated in the PCB by a pull-up resistor.

- Provide means for detecting the tri-state high impedance state in PCBs that utilize tri-state logic. The circuit of figure 4.3.3-2 is a detector for the high impedance level.



TRUTH TABLE

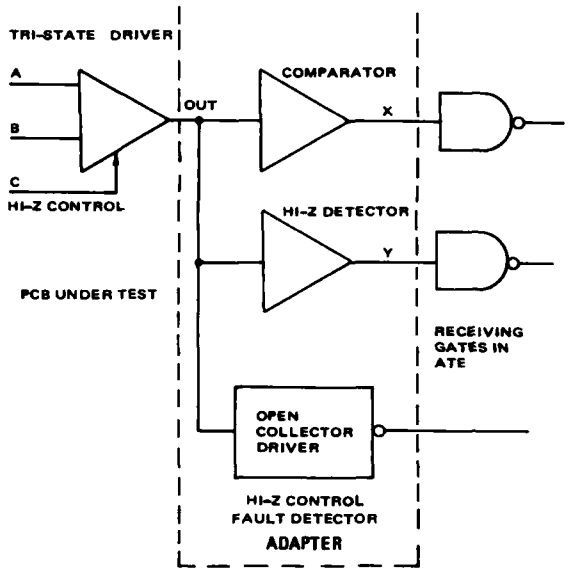
G1	G2
HIZ	0
0	1
1	1

Figure 4.3.3-2. Tri-State High Impedance State Detector

- To model the tri-state high impedance state, use a comparator and a tri-state high impedance detector in the adapter as shown in figure 4.3.3-3. The accompanying truth table shows the logic condition expected.

- When using tri-state circuits, use an open collector driver to inject data into the PCB under test as shown in figure 4.3.3-3. This prevents secondary failure in the Hi-Z detector if the Hi-Z control signal has faulted to a 0 when it should be a 1, a condition that can cause excessive current in the tri-state driver.

- Provide unique coding in the adapter and in the test software to prevent testing of an incorrect PCB with a given adapter. Also require the operator to enter the number of the PCBUT into the ATE via the keyboard to call up the correct test software. These precautions will prevent inadvertently damaging PCBs through use of an incorrect adapter and/or test program.



A	B	C	OUT	X	Y
0	0	0	0	0	1
0	1	0	1	1	1
1	0	0	1	1	1
1	1	0	1	1	1
X	X	1	HI Z	0	0

TRUTH TABLE

Figure 4.3.3-3. Tri-State Detection Circuit with Hi-Z Control Fault Protection

- Verify that each of the following functions is properly accommodated in the ATE/PCB interface adapter:
  - Stimulus/measurement buffering and routing
  - Passive loads and terminations
  - High frequency routing and transmission line characteristics/path length
  - High voltage/current/power routing
  - Digital message generation/reception
  - Noise pickup/feedback immunity

4.3.4 Test Fixture/Test Adapter Rules

4.3.4.1 General - The term test fixture or test adapter refers to the interface hardware between the ATE and the PCB under test (PCBUT). Some authorities include in this category general switching matrices and patchboards located in the ATE hardware. Others exclude all of the ATE hardware and include only the apparatus required to interface between the PCBUT and the ATE at its interface connectors. This paper presumes the latter point of view.

4.3.4.2 Rules of Adapter Design

- Interfacing is normally accommodated at two locations.
  - At a patch panel which allows interconnection of ATE stimulus/response lines to the I/O pins of the interface adapter in any combination. It often also includes patching of universal switch elements contained in the ATE.
  - In the interface adapter itself, to accommodate peculiar requirements of the PCB under test to the subset of universal capabilities of the ATE.
- The two important interface lessons to be learned.
  - Partition interface capability functionally by bandwidth.
  - Separate elements of stable technologies from those of changing technologies to avoid obsolescence of all due to the obsolescence of a part. Make functions dependent on changing technology easy to replace.
- Use the same manufacturing processes and quality controls for fabricating the adapters as are used for building the PCBs. Adapters are subject to very heavy use, hence should be built as well as a top-line product for a customer.
- Consider human engineering and safety aspects in the mechanical and electrical design of the adapter unit. Provide an accessible, solidly mounted test socket with adequate PCBUT access. Use quick disconnect I/O connectors located away from the adapter work area. Locate switches for easy access, indicators for high visibility. Cover all power connections, and ground the adapter to the ATE power ground. Allow room to access both sides of the PCBUT.
- Provide test points or I/O pins at outputs of sequential networks which are used to drive or provide input to memory devices.
- A useful way to ease the test generation problem for sequential circuits is to provide one test point, together with added logic elements. The test point is used to switch the circuit into a shift-register mode of operation, which is implemented by the additional logic.
- If the PCB is to be conformal coated prior to delivery, additional test points will be needed for field use since IC clips and probes can no longer make contact.

4.3.5 Modeling, Simulation and Automatic Test Program Generation[1]

4.3.5.1 Introduction - The complexity of LSI, VLSI and potential VVLSI logic elements makes it impossible to generate the required test vector patterns by hand. This has led to extensive use of computer simulation and analysis routines. These are used to model both simple and complex ICs, to interconnect them, and to generate the necessary test vectors to obtain the desired test coverage. The modeling routines usually consist of direct models of

- Use the simplest simulation that will provide access by the test generation program to all of the inputs and outputs of the logic element, including their timing relationships.

- The logic designer should be able to modify the model (under supervised controls) to conform to his application of the logic element. This modified model is then incorporated into the model file for that PCB.

- Unmodeled LSI devices are inevitable. When a model for an LSI chip cannot be devised (due to time or other constraints), use manual pattern generation to test the affected nodes. Merge these tests with tests generated using computer aids.

- Simulate microprocessors as functional devices using a Register Transfer Language rather than by gate level simulation. There is no true logical gate level equivalent for a microprocessor, it would require virtually unlimited memory, and stimulus/response times would be way too slow.[1]

- Alternatively simulate microprocessors using a chip level model as in figure 4.3.5-1. This model exhibits ease of generalization, has wide application to many system configurations, and has a reasonable level of complexity.

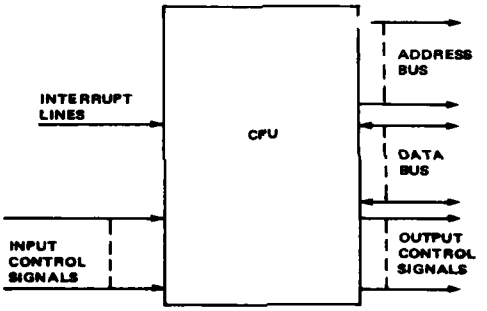


Figure 4.3.5-1. Chip Level Model of a Microprocessor

- A 4K semiconductor random access memory divides into five parts: (1) address decoders, (2) memory array, (3) data I/O bus, (4) sense amplifiers, (5) clock generator. See figure 4.3.5-2.

- A semiconductor read-only memory (ROM) has a similar block diagram, except that the write command (W) and the data-in signal (S) are not applicable.

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1. Selection Guide for Digital Test Program Generation Systems, Naval Ocean Systems Center Contract N00123-78-C-0333. 25 Oct 1978. This report is an excellent guide on available systems and their capabilities.

the IC devices by means of a device library. The analysis routines include the insertion of faults at the nodes of the modeled device. Faults normally simulated are stuck-at-one, stuck-at-zero; some simulation languages include simulation of delay times. These device simulation libraries, operational, and fault analysis routines are normally incorporated into the ATE so that it can be used both for generating the test programs and to test the PCBs.

The application of computers to automatic test program generation first requires a means of modeling all devices that may be encountered on a physical PCB, and a stored file of these devices that may be accessed by both the design and test engineers. Secondly it requires a means of interconnecting the device models to create a model of the PCB for which a test is to be generated. In the third place it requires a means of automatically generating a sequence of test vectors to stimulate the model of the PCB and to detect, store, and measure nodal activity resulting from the stimulus.

Fourth, such a system requires a means of measuring test comprehensiveness by ensuring that stimulation of virtually all of the nodes on the PCB can be uniquely detected at the I/O pins or at test points. Acceptable measures of test comprehension are judgmental decisions; they normally range from approximately 90% to over 98%, with the average about 95%. PC modeling, test vector generation and stimulation detection, and measurement of test comprehension is an interactive process that is continued until the desired test comprehension is attained. Manual test vector generation may be used to supplement automatic generation for final trimming to the desired level of test comprehension.

The fifth requirement for a complete system is a means of simulating fault conditions (stuck-at-1, stuck-at-0) at each node and the ability to detect these faults at the I/O pins or test points. More sophisticated systems also have the ability to simulate delay variances between stimulus and detection points, providing additional fault simulation capability. A final desirable capability of a test system is the ability to trace a fault from its point of detection at an I/O pin or test point to the faulty IC device. The design rules discussed in this section are aimed at achieving these objectives. The user is referred to the bibliographical references and footnote 1 for a complete, comprehensive, and up-to-date treatment of this subject.

4.3.5.2 General Design Rules

- Effective modeling of an IC device requires an understanding of its architecture and its functional operation.

- Gate level modeling is generally inadequate for large scale devices. Generally there is no true logic gate level equivalent. If a reasonable approximation can be devised it would require virtually unlimited memory to store the model. Stimulus and response times for such a large model would be excessively slow.

- Modeling of large scale devices can be effectively done with chip level modeling and the use of Register Transfer Languages,[1] (RTLs), particularly those that include the capability of fault simulation and detection.[1]

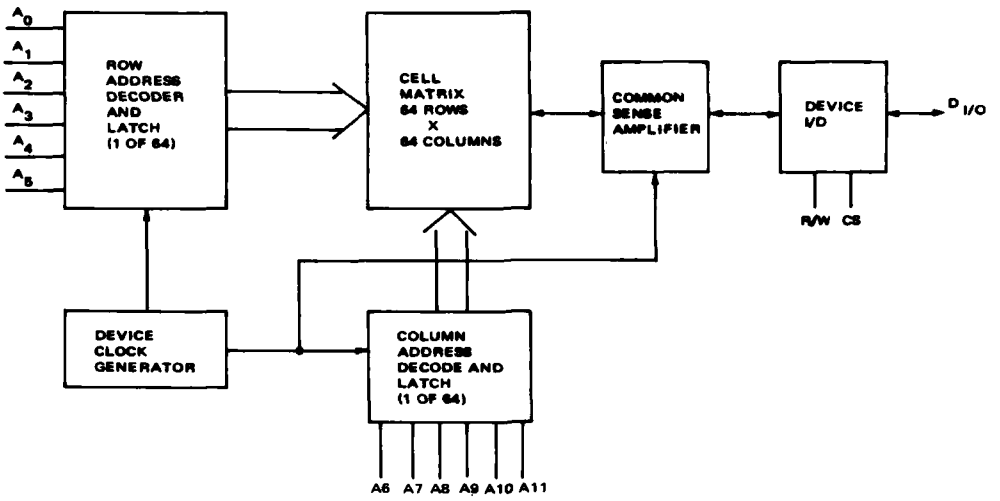


Figure 4.3.5-2. Block Diagram of 4Kx1 MOX Dynamic RAM

4.3.6 Maintenance Philosophy and Test Scenarios

4.3.6.1 General - The application of general testability design rules to a specific hardware usage situation requires consideration of the special conditions that surround that usage situation to make it unique. Among these conditions are the determination of what testing is to be done, and what levels of maintenance will support what kinds of testing. This, in turn, establishes the need for test and support equipment, material and spare parts, documentation, training, and personnel. These determinations are the task of the logistics system analyst; the result of his efforts is the logistics systems analysis and logistics support plan. As a gross example, certainly a card that is a "throw away" needs less designed in testability than one that is to be repaired. Hence the testability design must take into account the total maintenance philosophy and the test scenarios based thereon.

4.3.6.2 Aspects of Test Philosophy

- The object of testing is to verify the operability or nonoperability of the UUT. Once a PCB is determined to be faulty it must be repaired or discarded. To repair a card it is necessary to find the fault and to fix it. Testability must be designed into the card to optimize the ability to localize the fault to the defective component or wire etch, and to verify that the card is again ready for use. Serviceability must be designed into the card to optimize the ability to repair the defect at the repair center.

- Cost of test generation has been estimated as being proportional to the square of the number of logic nodes on a PCB. For logic networks with over 5,000 nodes, test generation is possible but very expensive; at 50,000 nodes using this measure it becomes prohibitively expensive. Partitioning into reasonably sized nodal groups either by electrical or mechanical means, thus subdividing the problem into manageable pieces, greatly reduces the complexity of test generation and hence its cost.

- There must be a continuing search for new algorithms and procedures to effectively test the developing large-scale devices of the present and future. There must also be thorough promulgation of new methods to ensure their rapid adoption and thorough evaluation in the arena of experience.

- Good testability is the result of considered design tradeoffs. Good testability doesn't just happen by accident, it must be designed in!

- The first step in defining a test program for a device is to fully understand the device. The second step is to divide the device into smaller coherent submodules and decide upon the order in which these should be tested in order to utilize the principle of expanding-on-the-kernel. The third step is to establish how the test system should be configured and used in order to implement the planned testing sequence.

- The very nature of large scale device implementation makes maintenance and testing a complex and time-consuming process.

- The most practical approach to the problem of testing complex PCBs is to utilize a segmented or structured test plan, in which various sections of the test are designed to seek specific types of potential faults. This approach permits dividing the testing problem into segments that allow most effective use of the variety of testing tools and techniques available to us in a state-of-the-art board test system.

- To effectively test large LSI/VLSI circuit cards, consideration must be given to test throughout the development of the logic. Choosing a test scenario is a part of the development of the logic itself. It is essential to know who will use the test, what equipment is available, spares availability, level of troubleshooting required, conditions under which testing is done, etc.

- The ideal situation is for engineering, factory, and field operations to all use compatible test systems. Then test programs can be generated by engineering and passed on to manufacturing test and to the field, undergoing updates, enhancements and feedback all the way. The use of ATLAS (Abbreviated Test Language for All Systems) promotes this universal compatibility. A less acceptable alternative is to provide software translators that will transform from the language of one test system to the test language of the other.

- Selection of the method for isolating failures is a system design decision. Two methods are in general use: (1) matching a failure to a fault dictionary of predetermined failures, (2) comparing the faulty PCB to a known good board (KGB) or gold board. The dictionary method requires large amounts of storage and sophisticated software to handle the data and make comparisons once the dictionary has been established. Data compression techniques are used to reduce the data storage requirements. Establishing and maintaining the integrity of a KGB or gold board has its own set of attendant problems.

- Failure mode verification requires that each potential failure be capable of being isolated to its source in order that, by its symptoms, it may be distinguished from all other potential sources of failure.

4.3.6.3 Designing the Test Procedure

- Use an automated design system for logic generation and card test development. Such systems provide automatic generation of test vectors, generate a dictionary of test results, automatically measure test coverage comprehensiveness, and facilitate making design changes to improve testability. They provide the means to completely design and test a PCB using software aids before a single element is committed to hardware. For a comprehensive study of such systems, see paragraph 4.3.5, footnote 1.

  - A preferred system structure is one that offers the ability to isolate components and prevent them from interacting with one another.

- Write general purpose self-test modules that apply to any system that is based on a particular microprocessor; for example, a CPU test module and a RAM test module. Usually only small changes are required to adapt these test modules from one system to another.

- Apply the principle of general purpose test modules to other repetitive logic patterns, where the test modules can be readily adapted from one system to another with only minor changes.

- The degree of testing of the prototype should be in inverse propotion to the maintainability estimate (mean time between repair actions) and in direct proportion to the number of PCBs of this unit to be built. Efforts to reduce service requirements should be in direct proportion to their anticipated need.

- Field failure data must be incorporated into the test process. Pattern sensitivities, such as to particular microprocessor instruction sequences, are most generally first detected in field applications.

- Shorten test sequence generation time and the resulting sequence by an ordered approach to test generation. For manual test generation the following steps can be applied:

  - Generate a list of all faults or fault combinations that may have sufficient frequency to be of importance. This is called a "fault list".

- Select a fault from the list and devise a test vector that will detect that fault. Find other faults in the fault list that are also detected by this pattern. Delete these from the fault list.

- Repeat the above process for each undetected fault on the list until a test vector has been found that will detect that fault. The resulting list of test vectors forms the test procedure for that PCB.

- This process can be used to establish coverage of automatically generated test vectors, and to manually implement an incomplete set (less than desired coverage) of automatically generated test vectors.

- Methods for finding an input pattern to detect a given fault include Roth's D Calculus[1] and the mathematical approach of Amar and Condulmari.[2]

4.3.6.4 Testing Prior to Functional Test

- Thoroughly test all LSI devices as IC packages before they are installed on a bare circuit board. Be especially attentive to applying this rule to microprocessor chips because of the great difficulty in performing adequate on-board testing.

- The objective of device testing is to sort and discard bad devices because they cannot be repaired. Economic considerations mandate the necessity of detecting bad devices at the earliest practical point in the test cycle.

- Test the bare printed wiring boards after etch and assembly to the connector for continuity, shorts, and opens, prior to assembly with components.

- The detection of shorts, opens, improper insertions, wrong components, etc, is most efficiently accomplished with in-circuit test systems prior to functional test.

4.3.6.5 Built-in Test/Self-Test

- Self-test is a useful concept in establishing good product testability. It is generally incorporated in the form of exercises and measurements performed by a product on itself to check out a significant portion of its circuitry. A typical sequence, which may be operator or self-initiated, results in a GO/NO-GO indication which may be made visible to the operator or detected by system confidence detection and control circuits.

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1. Roth, J.P., W.G. Bouricius, P.R. Schneider. "Programmed Algorithms to Compute Tests to Detect and Distinguish Between Failures in Logic Circuits." IEEE Trans. on Electronic Comp. Vol EC-16, Oct 67, pp 567-580.

2. Amar, V. and N. Condulmari, "Diagnosis of Large Combinational Networks." IEEE Trans. on Electronic Comp. (Short Notes) Vol EC-16, Oct 67, pp 675-680.

- o Incorporation of self-test capability into PCBs composed almost entirely of large scale ICs is a viable and powerful alternative to testing solely controlled by external ATE. Use of self-test macro sequences initiated from and controlled by the ATE program, combines the uniqueness of a dedicated self-test with the flexibility of an externally generated test.

- o Among the advantages that can accrue with an internal self-test are (1) operator intervention is bypassed, (2) a fault is isolated as soon as it occurs, (3) a fault can be isolated to a replaceable component, (4) system downtime is minimized.

- o Maintenance aids to incorporate into the design include built-in product-initiated self-tests and user-callable test. Self-initiated routines are automatically exercised by the product every time some preset condition is met. A user-callable routine is exercised only when the serviceman selects it.

4.3.7 Design Methods for Testability Improvement

4.3.7.1 General - Testability design for the 1980's, particularly the latter part, is expected to incorporate one or more of the specific design methodologies that attacks the problem at its source, the design of the IC chip itself. R. P. Davidson in a recent editorial in Electronic Test states[1]: "Chips have already been designed that were never manufactured because the design outpaced the existing test technology." This kind of problem will continue to exist and will become more common until testability characteristics are designed into the chip, not merely added on during PCB design - if then! Therefore, a brief review of some of the proposed approaches to this problem is included in this document.

The reason that testability has become an increasingly complex problem over the past few years is due to the rapidly increasing amount of logic on the PCBs and in the chips themselves. Conventional edge-pin testing is virtually obsolete for PCBs with a high LSI/VLSI count. Such cards also have high initial cost, high mean time to repair, and complex, expensive-to-develop test requirements. At the same time, management demands are for shorter tests, more rapid localization of errors to a faulty component or foil defect, and a reduction of the spare card pipeline. Stewart sums up the problem thus[2]: "The situation has created an industry-wide need for the development of comprehensive, innovative fault test scenarios that go far beyond simply enhancing fault detection software and trying to test cards after they are built."

The design methodologies reviewed herein, and others presented in the literature, are an attempt to solve these problems in a positive manner. The goal of these methods is to reduce the cost of testing. The consensus seems to be that this is best done by transforming sequential networks into combinational equivalent networks. This implies that the problem is most completely approached at the chip design level, since it is here that the logic is concentrated.

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1. Davidson R.P, Bell Laboratories, Murray Hill, N.J., "Testing VLSI Boards, Can We Meet the Challenge?" Electronic Test, May 1979, p 6.

2. Stewart J.H., Sperry Univac, Roseville, Minn., "Future Testing of Large LSI Circuit Cards", p 36.

The logic design techniques must be coupled with a means of automatic test vector generation during the test to significantly reduce the test set memory requirements for stimulation vector storage. Coupled with this must be a method of test result vector compaction to a length economical to store efficiently in a data dictionary. This three-pronged approach holds great promise of some day reducing the problem of test development and performance to manageable size.

Signature analysis is the most logical candidate to use for data compaction. If a 20-bit register is used, the probability of an erroneous result is less than one part per million - certainly an acceptable risk in view of the benefits gained. The technique is easy to implement as part of the tester. Also important, is that it employs the same logical structure and mathematical characteristics as a pseudorandom number shift-register generator.

Significant work has also been done in the field of automatic on-line test vector generation. A number of different algorithms have been developed and are in use today. The topics of algorithm development, analysis, and implementation form a significant field of study in computer science. It is beyond the scope of this document to probe into this area; however, a number of papers in the bibliography deal with specific aspects of the problem.

One of the major fields of testability research involves the problem of how to make testable PCBs that contain a number of large scale devices and significant sequential logic. As some of the papers reviewed indicate, the more comprehensive proposals are directed to both chip and PCB design. There are also a number of papers in the bibliography that deal with this topic, several of which are reviewed below. Special reference is made to Stewart's paper[2] from which figure 4.3.8-2 has been adopted.

4.3.7.2 Data Compaction Methods

- The paper "Testing Logic Circuits with Compressed Data" by H. Fujiwara and K. Kinoshita presents theorems showing that various data compression methods in common use require twice the number of tests so that true compaction is not realized. It presents test schemes, backed by theorems, that provide logarithmic (base 2) compression of response data without increasing the number of tests, and a scheme, again backed by theorems, providing compression of response data to 2 bits regardless of the number of tests by adding only two tests. A relatively effective scheme for test result compression is then presented. The ten theorems on data compression and testing are applicable only to combinational networks.

- Signature Analysis (SA) is discussed by several papers in the bibliography. It is a method of data compaction based on the mathematics of pseudorandom number generation using a shift register and feedback. The technique is illustrated in figure 4.3.7-1. The reference values are developed from a known-good-board, or a simulation of the board is used to develop both the test vector sequences and the "good board" signatures.

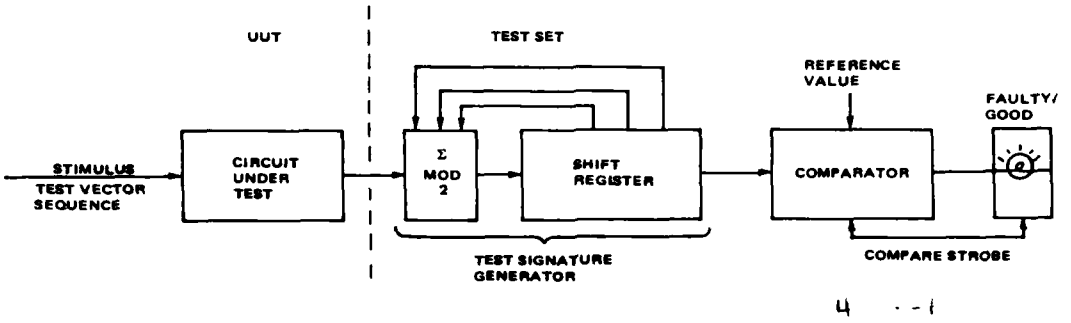


Figure 4.3.4-1. General Testing Scheme Applying Signature Analysis Testing Method

Signature analysis is more than just a data compaction method, it also involves the application of a test philosophy and a test secenario to make the results significant and useful. As conceived by several authors, it is most applicable to LSI/VLSI and microprocessors where the stimulus can be provided by the product itself, and where partitioning can be employed to allow testing of selected circuit portions independent of others. The technique can be combined with "expansion on the kernel" to test microprocessor based products. For products that cannot provide their own stimulus, the test vectors must be provided externally. This implies combining signature analysis with a means of automatic test vector generation. Proper application of the SA technique implies careful analysis to ensure that valid, meaningful signatures are obtained, which, in turn, implies a firmly established discipline of testing application technology.

4.3.7.3 Fault Modeling

- The paper "Fault Simulation Strategy for Combinational Logic Networks" by S. J. Hong combines known techniques of fault simulation with new techniques to develop a fault simulation strategy optimized to the size and structure of a given combinational network. This new approach partitions the structure into fanout-free regions (FFR) terminating in fanout stems (FOS). The resulting tree networks are analyzed by a variation of deductive simulation that reduces faults to a near minimal equivalent single fault set (SFS) generated by the new simple way presented. Theorem 1 proves that the SFS represents all single stuck faults in the network. Theorem 2 proves two conditions of live fault testing in the tree network. Theorem 3 proves two conditions of fault testing for an FFR. The testing

strategy and simulation algorithm are presented in detail. Savings are realized by the simple fault set construction method, reduction to only two passes and very reduced storage requirements. The method apparently can also be applied to multiple output networks.

- The text "Diagnosis and Reliable Design of Digital Systems" by M. A. Bruer and A. D. Friedman, and Dr. Bruer's studies for Hughes Aircraft Company on "Modeling (Faulty Digital Circuits)" and "Digital Logic Simulation" also discuss aspects of fault modeling. Other papers are cited in the bibliography.

4.3.7.4 Test Design Methods

- Six papers by IBM staff engineers (1,2,3,4,5,6) describe a new test methodology for LSI/VLSI systems, and how a system incorporating the methodology was designed and implemented. The first paper gives background data, tells what solution was reached, and briefly outlines the means of implementation.

  The second paper describes a logic structure that uses level sensitive design to eliminate rise, fall, and delay time dependence. It unites all storage elements into shift registers by a form of scan/set methodology to transform sequential logic into combinational logic, which simplifies test generation applicable to LSI design. The technique is effective because it has low sensitivity to AC design parameters. Control of input clocks and delays is the major concern of level sensitive design, requiring the use of a level-sensitive polarity hold latch for storage. Arranging these latches into shift registers more than doubles the required logic. Specific design rules for clock and timing must be implemented. The overall combination of level sensitive design and scan shift registers, called level sensitive scan design (LSSD), eliminates hazards and races to greatly simplify fault simulation and testing. The circuits act as combinational networks, hence well known combinational test techniques can be applied using scan/set testing principles. Circuit performance is dependent only on path delay being less than a preselected value. Note that implementation requires that the LSI/VLSI chips be designed using the special latch.

  The third paper gives a method of automatically checking for compliance of logic structures to the design ground rules presented in the second and third papers. The fourth paper describes a system of automatic test pattern generation for large logic networks built according to the design rules of papers 2 and 3. Paper four also gives an algorithm for automatically generating delay tests for such logic nets. The last paper presents a means of simulating delay lists and determining which delay faults have been detected.

  From the papers it appears that at the least experimental SI/VLSI packages using the described design methodology have been developed. However such chips are not available on the market, nor does it appear that they will be in the foreseeable future.

1. M. Correia and F. B. Petrini, "Introduction to an LSI Test System."

2. E. B. Eichelberger and T. W. Williams, "A Logic Design Structure for LSI Testability."

3. H. C. Godoy, P. S. Bottorff, C. G. Franklin, "Automatic Checking of Logic Design Structures for Compliance with Testability Ground Rules."

4. P. S. Bottoroff, R E. France, N. H. Garges, E. J. Orosz, "Test Generation for Large Logic Networks."

5. E. P. Hsieh, R. A. Rasmussen, L. J. Vidunas, "Delay Test Generation."

6. T. M. Storey and J. W. Barry, "Delay Test Simulation."

- The paper "Future Testing of Large LSI Circuit Cards" by J. H. Stewart compares five test scenarios after describing some of their major subdivisions. First is built-in-test, which subdivides into hardware BIT, software BIT, and the selected combination of them, called microdiagnostics. Second is drive/sense (bed-of-) nails. Third is sense only nails stimulated by edge (I/O pin) drive. Fourth is edge drive/sense. Fifth is scan/set which provides a data path out of the card via added logic and output pins separate from the functional logic; the purpose is to expose internal nodes of a chip or PCB for test purposes. The two common forms of scan, bit-serial using a shift register, and multiplex are described. The shift register form allows both scan of results and set(ing) of input vectors. The types of nodes that should be scanned are listed. Rules for good testability design also apply when using the scan/set concept. A comparison of test system characteristics using the five scenarios is included in this summary as figure 4.3.7-2 because it illustrates the capabilities available for the intermediate term future.

- M. A. Bruer and M. Abramovici in a presentation at Hughes Aircraft Company, Ground Systems Group pointed out that though scan/set is most effective in terms of testability improvement when applied at the chip design, its use at the PCB design level also can be of significant benefit. This point is also discussed in Bruer's private correspondence with Hughes Aircraft Company, "Design for Testability."

4.3.8 Management for Testability

4.3.8.1 General - An effective testability program requires active management support. Management establishes the program policies, a subset of which is the policy and philosophy governing testability. The manager assigns the responsibilities, but is also responsible for their execution. He controls the attitudes of his people by his own attitude and that of his senior staff members. His people will consider important what he, by action, considers important, and unimportant what he demonstrates to be unimportant. The specific responsibilities and tools of management in general naturally apply here. However there are also some clear guidelines that relate directly to the requirements placed on management to ensure an effective testability program. A selection of the more important of these guidelines are included in this study.

TEST SYSTEM CHARACTERISTICS	TEST SCENARIO					
	DESIGN PCB FOR BIT USING MICRODIAGNOSTICS	DRIVE/SENSE BED-OF-NAILS	EDGE PIN STIMULUS COMBINED WITH BED-OF-NAILS SENSE ONLY	STIMULUS AND SENSE AT EDGE PINS ONLY	EDGE PIN WITH PCB DESIGNED FOR SCAN/SET
TEST TIME REQUIRED	FEW SECONDS	FEW MINUTES	FEW SECONDS	FEW SECONDS	FEW SECONDS
FAULT RESOLUTION. FAULT RESOLVED TO- COMMENTS	VERY HIGH. NORMALLY TO FAILING CHIP- ADDITIONAL CONTROL NEEDED TO RESOLVE CHIPS ON A BUS	VERY HIGH RESOLUTION OF CHIP FAILURES. FOIL NOT CHECKED WELL- PRETEST PBW AS BACKUP	HIGH RESOLUTION. TO CHIP OR BUS NODE- ALSO CHECKS FOIL.	LOW RESOLUTION. TO EXTERNAL NODE-	HIGH RESOLUTION. TO CHIP OR BUS NODE-
RELIABILITY OF TESTER	NO TESTER REQUIRED. MUST HAVE PROCESSOR ON PCB TO RUN BIT	LOW MODERATE	HIGH MODERATE	HIGH	HIGH
SOFTWARE DEVELOPMENT COST	NOMINAL	NOMINAL	HIGH	HIGH	HIGH
TEST GENERATION COST/MANPOWER AND COMPUTER TIME.	NOMINAL	NOMINAL	HIGH	VERY HIGH	HIGH
EASE OF TEST UPDATE	EXCELLENT. ONLY NEEDED TO MODIFY BUILT-IN DIAGNOSTIC PROGRAM	GOOD. INTERCONNECTION BETWEEN CHIPS IS OF MINOR IMPORTANCE. FOR NEW CHIPS ADD A NEW FUNCTIONAL TEST TO EXISTING PACKAGE	POOR. EDGE PINS USUALLY REQUIRE A WHOLE NEW TEST IF ANY PART OF THE CARD IS CHANGED.		
COST TO REPRODUCE THE TESTER	NONE. NO TESTER REQUIRED	VERY HIGH	HIGH	NOMINAL	NOMINAL
TEST DATA BASE SIZE. COST COMMENTS	SMALL. LOW, VERY INFREQUENT UPDATES. EASY TO DO USING MICRODIAGNOSTICS	SMALL TO MODERATE. NOMINAL, FREQUENT UPDATES. ONE TEST PER CHIP TYPE	LARGE. HIGH. FREQUENT UPDATES.		
DESIGN GUIDELINES AND CONSTRAINTS ON PCBUT (IMPACT ON COST AND/OR PERFORMANCE (C/P)	MUST INCLUDE BIT IN HARDWARE AND SOFTWARE. SEVERE C/P IMPACT. VERY STRONG CONSTRAINTS	BOARD LAYOUT AND PARTS LOCATION CONSTRAINTS. SLIGHT C/P IMPACT. MODERATE CONSTRAINTS	BOARD LAYOUT AND PARTS LOCATION CONSTRAINTS. SLIGHT C/P IMPACT. LOW MODERATE CONSTRAINTS	C/P IMPACT MAY BECOME PROHIBITIVE IN LARGE LSI. MILD CONSTRAINTS	SPECIFIC CONSTRAINTS TO INCORPORATE SCAN/SET INTO DESIGN. NOMINAL C/P IMPACT. STRONG CONSTRAINTS
ABILITY TO TEST AT HIGH SPEED	HIGH	HIGH	NOMINAL	NOMINAL	NOMINAL

Figure 4.3.7-2. A Comparison of Test S
Using Five Different Test

AME SIZE

△ Information Media Department
Standard MODULAR Keyline
NOTE: RIGHT HAND FOLDOUT

Proof | Ink | Art | CRC | Log No | Vol. N

12-489 4/1/70

Vendor's Name _____

TESTER	MUST HAVE PROBES ON PCB TO RUN BIT					
SOFTWARE DEVELOPMENT COST	NOMINAL	NOMINAL	HIGH	HIGH	HIGH	HIGH
TEST GENERATION COST/MANPOWER AND COMPUTER TIME.	NOMINAL	NOMINAL	HIGH	VERY HIGH	HIGH	HIGH
EASE OF TEST UPDATE	EXCELLENT. ONLY NEEDED TO MODIFY BUILT-IN DIAGNOSTIC PROGRAM	GOOD. INTERCONNECTION BETWEEN CHIPS IS OF MINOR IMPORTANCE. FOR NEW CHIPS ADD A NEW FUNCTIONAL TEST TO EXISTING PACKAGE	POOR. EDGE PINS USUALLY REQUIRE A WHOLE NEW TEST IF ANY PART OF THE CARD IS CHANGED.			
COST TO REPRODUCE THE TESTER	NONE. NO TESTER REQUIRED	VERY HIGH	HIGH	NOMINAL	NOMINAL	NOMINAL
TEST DATA BASE SIZE. COST COMMENTS	SMALL. LOW, VERY INFREQUENT UPDATES. EASY TO DO USING MICRODIAGNOSTICS	SMALL TO MODERATE. NOMINAL, FREQUENT UPDATES. ONE TEST PER CHIP TYPE	LARGE. HIGH. FREQUENT UPDATES.			
DESIGN GUIDELINES AND CONSTRAINTS ON PCBUT (IMPACT ON COST AND/OR PERFORMANCE (C/P)	MUST INCLUDE BIT IN HARDWARE AND SOFTWARE. SEVERE C/P IMPACT. VERY STRONG CONSTRAINTS	BOARD LAYOUT AND PARTS LOCATION CONSTRAINTS. SLIGHT C/P IMPACT. MODERATE CONSTRAINTS	BOARD LAYOUT AND PARTS LOCATION CONSTRAINTS. SLIGHT C/P IMPACT. LOW MODERATE CONSTRAINTS	C/P IMPACT MAY BECOME PROHIBITIVE IN LARGE LSI. MILD CONSTRAINTS	SPECIFIC CONSTRAINTS TO INCORPORATE SCAN/SET INTO DESIGN. NOMINAL C/P IMPACT. STRONG CONSTRAINTS
ABILITY TO TEST AT HIGH SPEED	HIGH	HIGH	NOMINAL	NOMINAL	NOMINAL	NOMINAL
ABILITY TO TEST CARDS CONTAINING LSI, VLSI, VVLSI	HIGH	MODERATELY HIGH	LOW	VERY LOW	MODERATE IF SCAN/SET IS USED ON PCB ONLY. HIGH IF SCAN/SET IS BUILT INTO LSI	
CONSTRAINTS ON TEST METHODOLOGY/ TEST PROCEDURE DEVELOPMENT	VERIFY THE KERNEL, THEN EXPAND ON IT	BASICALLY A SET OF CHIP TEST ROUTINES	NEED A MEANS OF AUTO TEST VECTOR GENERATION AND COMPACTION OF RESULTS-DATA FOR PCB'S WITH SIGNIFICANT QUANTITY OF LSI			

Figure 4.3.7-2. A Comparison of Test System Characteristics Using Five Different Test Scenarios

Information Media Department Standard MODULAR Keyline NCTE: RIGHT HAND FOLDOUT	Proof	Ink	Art	CRC	Log No. 99-2 Vol. No.

12-489 4/1/80

Vendor's Name _____

4.3.8.2 General Management Considerations

- The test systems introduced most successfully into the Navy have been those for which the workload and application have been planned in advance and used as a basis for system design. This includes general purpose ATE which was tailored to meet the intended application.

- Systems that are most accepted by both test program designers and test operators are those with an interface of straightforward and conservative design.

- Digital and RF Capabilities and requirements have "turned over" every one to three years, with each new weapon system outstripping available capability in digital and RF areas. This implies the need for partitioning to segregate the volatile and stable technologies so that modifications to incorporate the latest technology can be more readily implemented.

- Incorporate design for testability directly into the system design philosophy and make each circuit designer responsible for the testability design of his circuits. We can no longer afford the luxury of separate design and test activities, with divided responsibility.

- One study group came to the conclusion that only the logic designer understood the logic configuration, therefore only he could develop the logical test patterns required. For large, complex networks these patterns are seemingly endless.

- The lead designer of the PCB must be responsible for making sure that the logic design and the hardware configuration are compatible with good testability practices.

- Managers are reluctant to have their top logic designers devote a significant percentage of their time improving the testability of an existing design, when that same time can be employed in developing new designs.

- Assign test engineer specialists to review each card design and recommend means for improving its testability to attain the required test comprehensiveness. Give him veto authority over the design so that he can block its release until the testability goals have been achieved. The program manager retains his usual authority to resolve deadlocks.

- Testability criteria should be evaluated by an engineer experienced in the disciplines of PCB testing and repair.

- Assign the entire PC card test development package, test adapter, test program, and supporting documentation to the same test engineer. This pinpoints responsibility.

- Require utilization of a computer-aided design system that has the following characteristics: (1) ability to generate a testability profile on each PCB as it is designed, (2) an automatic test generation capability for all PCBs built using the systems' IC library. (This is not an exhaustive list of required characteristics.)

- Control the amount of test documentation generated to provide adequate coverage for the particular program needs. This is a judgmental decision. Too little documentation results in inefficiencies and the need for PhD technicians, too much and the resources are overburdened to the point of breakdown or avoidance.

- Maintain a testability profile on each card through its development. The test engineer for the PCB has the responsibility for maintaining the profile. Figure 4.3.8-1 is a suggested format for the testability profile.

- Schedule adapter development on the basis of reliability estimates and total production. Divide card type MTBF by total production for that card type. Schedule adapter development in increasing order of the resultant.

- Provide one adapter of each type for each production test station that will be testing that card type. This allows multiple testing of the most used card types.

DIGITAL PCB TESTABILITY PROFILE PART NO.

CARD DESIGN PHASE	SIMULATION			FIRST ARTICLE	FACTORY	FIELD
TESTABILITY ANALYSIS RUN NUMBER/OR ACTUAL TEST RUN	CARD DEVELOPMENT			UPDATE 1	UPDATE 2	UPDATE 3
	TRIAL 1	TRIAL 2	TRIAL 3			
PERCENT TESTED						
AVERAGE NUMBER OF ICs PER FAULT SIGNATURE						
NUMBER OF FAULT SIGNATURES THAT DO NOT ISOLATE TO 3 OR LESS ICs						
COMPUTER TIME REQ'D TO GENERATE OR RUN TEST						
MANUAL PROMPTING MANHOURS						

Figure 4.3.8-1. Digital PCB Testability Profile

4.3.8.3 Testing Goals

- The basic testing goal is to isolate a failure to a failing chip or foil. To reach this goal, establish the following sub-goals.

  - Enforce the application of the testability design guidelines prior to any attempt to develop a test for a PCB. This should drastically reduce PCB redesign time required to meet the minimum-percent-tested requirement. A testability design review is essential.

    Establish a minimum requirement for percent of card tested as measured by the card test software simulator. Use nodal fault simulation (stuck-at-one/stuck-at-zero) so that tests developed for the factory will also serve the field.

  - Require faults to be resolved to the failing chip. For each fault, record the fault node tree including terminal nodes (I/O pins and test points) associated with the input test vector. Record the transition count signature expected at each node of the tree. Limit the average and maximum number of nodes per fault node tree.

  - Establish maximum computer and manpower time limits for test trimming using manual test vector generation techniques.

  - Establish a fault resolution profile for each PCB. This should consist of (1) an average maximum number of chips to which a fault must be isolated, designated n_i; (2) the percentage of faults isolated to one chip; (3) the differential percentage isolated to two chips; (4) ...and so on up to n_i; and (5) the differential percentage of faults isolated to more than n_i chips. Measure, record, and maintain a fault resolution profile for each PCB.

4.3.9 Bibliography

4.3.9.1 General - Many sources from the literature and significant Hughes Aircraft Company experience and research were used in developing this set of testability design guide rules. Significant contributions were obtained from the papers listed in the bibliographies both for background and as direct contributions. Due to the multiple sources for many of the rules, direct credit is difficult to assign, except in the specific instances cited in the text.

The bibliography is arranged in general in the same manner as the body of the report but with more divisions. It begins with general rules and concludes with management guidelines. For the most part, each paper has been classified into a single category, its major area of contribution. Secondary classifications, with a few important exceptions, have been omitted. Textbooks have been grouped into a single category because they normally consider in a single document a number of the different subtopics of testability.

This bibliography is by no means exhaustive. The texts and many of the papers contain significant bibliographies of their own, some of which were used as sources for additional papers for this report. For the most part papers prior to 1970 were arbitrarily omitted. Time did not permit the culling that should properly be done for selecting from among these older papers.

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3-75	Data Word Manipulation	6-23-75	3
4-75A	Memory Board Error Mapping	9-25-75	8
1-78	Hardware Versus Software Board Error Mapping	Feb 78	2
1-77	Increasing Throughput of the Adar DR 12/25 with Board Error Mapping (BEM) and ATLS12/25	Jan 77	6
2-77	ROM Testing on the DR12/25 - The Comparison Method	May 78	5
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SECTION IVC
TESTABILITY IMPROVEMENT

5.0 Subtask: Testability Improvement of Benchmark PC Cards

5.1 General Considerations

5.1.1 Purpose - The purpose of this subtask is to examine the testability of the MIRADCOM benchmark PCBs and, in line with the results of the study, make recommendations for improving their testability.

5.2 Format of the Testability Evaluation

5.2.1 Report Divisions - The PCB testability evaluation is divided into three parts: general recommendations, specific recommendations, and expected testability improvements.

5.3 Testability Recommendations

5.3.1 General Recommendations Applicable to MIRADCOM Cards

- CARD TYPES:

  390037 DIGITAL AUTOPILOT NO. 1
  390038 DIGITAL AUTOPILOT NO. 2
  390039 DIGITAL AUTOPILOT NO. 3
  390040 DIGITAL AUTOPILOT NO. 4

- CONDITION: Digital autopilot cards do not make use of available test points.

  ACTION: Use test points at vital signal, control, I/O, or power lines.

- CONDITION: Not all intermodule connections are available to the test set.

  ACTION: Provide edge connector pins for data bus, address bus, and control line interconnections. Alternatively, provide jumpers to permit opening bus and control lines between modules.

- CONDITION: Logical inputs are not accessible for test set control of the logic state when tied directly to a high logic reference.

  ACTION: Where required, apply a logic high to element inputs through a pull-up resistor instead of direct 5VDC, except for low power Schottky devices.

5.3.2 Specific Recommendations

5.3.2.1 390037 DIGITAL AUTOPILOT NO. 1

- CONDITION: Oscillator cannot be disabled or bypassed.

  ACTION: Use a gate to provide edge connector access.

- CONDITION: (390007 module) The clock line into IC1 is not accessible.

  ACTION: Use an edge connector pin or a gate to reset, disable, or provide an external clock from the test set.

- CONDITION: (390007 Module) Fan-out points from IC3 (pins 12, 13) are not accessible.

  ACTION: Provide test points for test monitoring.

- CONDITION: (390007 Module) Eleven input signals that form the input to IC2 are not accessible at any input nodes. IC2 performs the "OR" function and a faulty signal input can go undetected because of IC2's internal logic connections.

  ACTION: Provide separate "OR" gates, test points, or edge connector pins for IC2 input nodes. Use explicit, separable logic at IC pins for equivalent gating in place of 7464 chip.

- CONDITION: (390025 Module) NAND gates are WIRE-ANDed.

  ACTION: Use a gate, test points, or edge connector pins to simplify test.

- CONDITION: (390027 Module) Output of IC5, pin 8, is not accessible and is tied to IC1, IC2, IC3, IC4, IC5, and IC6.

  ACTION: Use test points, edge connector, or gating to provide test access to this signal.

5.3.2.2 390038 DIGITAL AUTOPILOT NO. 2

- CONDITION: (390004 Module) Preset and clear are tied together to 5V on IC6.

  ACTION: Use separate pull-up resistors to apply logic high to preset and clear inputs.

- CONDITION: (390004 Module) Each of four, 4-bit microprocessor chips cannot be individually tested.

  ACTION: Provide gates and edge connector pins allowing test set access to all input and output lines independently of the other microprocessor chips.

- CONDITION: (390031 Module) Feedback loop from PROMs (IC1, IC2, IC3) to register (IC4) does not permit test access.

  ACTION: Provide gates at PROM outputs to allow external control of the loop at the edge connector pins.

5.3.2.3 390039 DIGITAL AUTOPILOT NO. 3

- CONDITION: (390016, 390019 Modules) Multiplexer outputs (IC2, IC3, IC4, IC5) to buffer register (IC1) are not accessible.

  ACTION: Provide gates and edge connector pins to allow test set access to multiplexer outputs.

- CONDITION: (390044 Module) S/L input to shift register (U4) from NAND gate (U9) is not accessible.

  ACTION: Provide gates to control U4 at the edge connector.

- CONDITION: (390044 Module) Feedback loop from U2 to U7 does not permit test access.

  ACTION: Provide gates at node to allow external control of loop at the edge connector pins.

- CONDITION: (390044 Module) Enable and load inputs to counters (U1, U2, U3) do not permit test set access.

  ACTION: Where required, apply a logic high to enable and load inputs through a pull-up resistor. Provide access to all enable and load inputs at edge connector pins.

- CONDITION: (390044 Module) Clear input to flip-flop (U6) does not permit test set access.

  ACTION: Provide gates to allow external control of flip-flop at edge connector pin.

5.3.2.4 390040 DIGITAL AUTOPILOT NO. 4

- CONDITION: (390010, 390051 Modules) All logic high inputs are tied directly to 5VDC.

  ACTION: Apply logic high through pull-up resistors for elements V1, T1, IC6.

- CONDITION: (390051 Module) Binary counters (V1, T1) and up/down counters (V2, V3, V4, V5, T2, T3, T4, T5) do not permit test access.

  ACTION: Provide gates to partition counter chains with external control lines at edge connector pins (see figure 5.3-1).

  ACTION: Provide gates for "UP/DOWN," "LOAD," and "ENABLE" inputs to control each up/down counter at the edge connector pins.

  ACTION: Provide "WIRE-AND" connections at "ENABLE" and "LOAD" inputs to control the binary counters at the edge connector pins. (See figure 5.3-2)

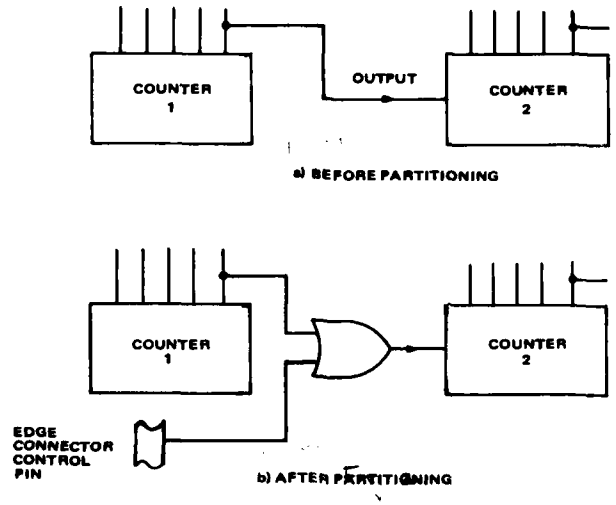
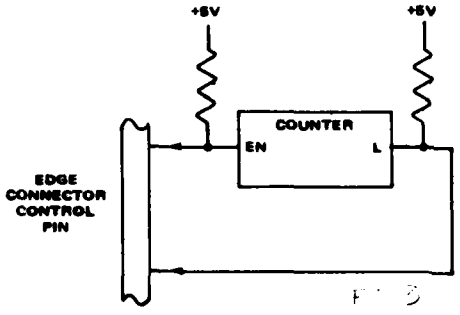


Figure 5.3-1. Provide gates to partition counter chains.



NOTE: Do not tie "enable" and "load" inputs together.

Figure 5.3-2. Provide WIRE-AND at enable and load inputs.

- CONDITION: (390010 Module) Tri-state buffers are WIRE-ANDed together.

  ACTION: Partition fan-out into smaller groups and provide access to "WIRE-AND" nodes at edge connector pins.

5.3.3 Testability Improvement for MIRADCOM Digital Autopilot PCB's - The testability projections shown below may be realized by incorporating the preceding recommendations into the digital autopilot PCB's.

5.3.3.1 DIGITAL AUTOPILOT NO. 1 (390037)

Present Testability[1]	75%
Projected Testability	90%

5.3.3.2 DIGITAL AUTOPILOT NO. 2 (390038)

Present Testability	80%
Projected Testability	92%

5.3.3.3 DIGITAL AUTOPILOT NO. 3 (390039)

Present Testability	60%
Projected Testability	90%

5.3.3.4 DIGITAL AUTOPILOT NO. 4 (390040)

	Digital Portion	Overall
Present Testability	.70	42%
Projected Testability	.91	55%

* NOTE: This PCB contains 60% digital and 40% analog circuitry. Testability percentages refer to overall testability.

[1]Testability is defined as the ability to perform a functional test on all elements at card connector.